

Summary

The Xilinx® Kintex® UltraScale+™ FPGAs are available in -3, -2, -1 speed grades, with -3E devices having the highest performance. The -2LE and -1LI devices can operate at a V_{CCINT} voltage at 0.85V or 0.72V and provide lower maximum static power. When operated at a V_{CCINT} voltage at 0.72V, the -2LE and -1LI performance and static and dynamic power is reduced. However, when operated at a V_{CCINT} voltage of 0.85V using -2LE and -1LI devices, the speed specification for the L devices is the same as the -2I or -1I speed grades with reduced static power.

DC and AC characteristics are specified in extended (E) and industrial (I) temperature ranges. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade extended device are the same as for a -1 speed grade industrial device). However, only selected speed grades and/or devices are available in each temperature range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This data sheet, part of an overall set of documentation on the Kintex UltraScale+ FPGAs, is available on the Xilinx website at www.xilinx.com/documentation.

DC Characteristics

Table 1: Absolute Maximum Ratings⁽¹⁾

Symbol	Description	Min	Max	Units
FPGA Logic				
V_{CCINT}	Internal supply voltage.	-0.500	1.000	V
V_{CCINT_IO} ⁽²⁾	Internal supply voltage for the I/O banks.	-0.500	1.000	V
V_{CCAUX}	Auxiliary supply voltage.	-0.500	2.000	V
V_{CCBRAM}	Supply voltage for the block RAM memories.	-0.500	1.000	V
V_{CCO}	Output drivers supply voltage for HD I/O banks.	-0.500		V
	Output drivers supply voltage for HP I/O banks.	-0.500		V
V_{CCAUX_IO} ⁽³⁾	Auxiliary supply voltage for the I/O banks.	-0.500	2.000	V
V_{REF}	Input reference voltage.			V
V_{IN} ⁽⁴⁾⁽⁶⁾⁽⁷⁾	I/O input voltage for HD I/O banks ⁽⁵⁾ .	-0.500		V
	I/O input voltage for HP I/O banks.	-0.550	$V_{CCO} + 0.550$	V
V_{BATT}	Key memory battery backup supply	-0.500	2.000	V

Table 1: Absolute Maximum Ratings⁽¹⁾ (Cont'd)

Symbol	Description	Min	Max	Units
I_{DC}	Available output current at the pad.			mA
I_{RMS}	Available RMS output current at the pad.			mA
GTH or GTY Transceiver				
$V_{MGTAVCC}$	Analog supply voltage for the GTH or GTY transmitter and receiver circuits.	-0.500	1.000	V
$V_{MGTAVTT}$	Analog supply voltage for the GTH or GTY transmitter and receiver termination circuits.	-0.500	1.300	V
$V_{MGTVCCAUX}$	Auxiliary analog Quad PLL (QPLL) voltage supply for the GTH or GTY transceivers.	-0.500	1.900	V
$V_{MGTREFCLK}$	GTH or GTY transceiver reference clock absolute input voltage.	-0.500	1.300	V
$V_{MGTAVTTRCAL}$	Analog supply voltage for the resistor calibration circuit of the GTH or GTY transceiver column.	-0.500	1.300	V
V_{IN}	Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage.	-0.500	1.200	V
$I_{DCIN-FLOAT}$	DC input current for receiver input pins DC coupled RX termination = floating.	-		mA
$I_{DCIN-MGTAVTT}$	DC input current for receiver input pins DC coupled RX termination = $V_{MGTAVTT}$.	-	0 ⁽⁸⁾	mA
$I_{DCIN-GND}$	DC input current for receiver input pins DC coupled RX termination = GND.	-	0 ⁽⁸⁾	mA
$I_{DCIN-PROG}$	DC input current for receiver input pins DC coupled RX termination = programmable.	-	0 ⁽⁸⁾	mA
$I_{DCOUT-FLOAT}$	DC output current for transmitter pins DC coupled RX termination = floating.	-		mA
$I_{DCOUT-MGTAVTT}$	DC output current for transmitter pins DC coupled RX termination = $V_{MGTAVTT}$.	-		mA
System Monitor				
V_{CCADC}	System Monitor supply relative to GNDADC.	0.500	2.000	V
V_{REFP}	System Monitor reference input relative to GNDADC.	0.500	2.000	V

Table 1: Absolute Maximum Ratings⁽¹⁾ (Cont'd)

Symbol	Description	Min	Max	Units
Temperature				
T _{STG}	Storage temperature (ambient).	-65	150	°C
T _{SOL}	Maximum soldering temperature ⁽⁹⁾ .	-	260	°C
T _J	Maximum junction temperature ⁽⁹⁾ .	-	125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. V_{CCINT_IO} must be connected to V_{CCBRAM}.
3. V_{CCAUX_IO} must be connected to V_{CCAUX}.
4. The lower absolute voltage specification always applies.
5. If V_{CCO} is 3.3V, the maximum voltage is 3.4V.
6. For I/O operation, see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).
7. The maximum limit applied to DC signals. For maximum undershoot and overshoot AC specifications, see [Table 4](#) and [Table 5](#).
8. For more information on supported GTH or GTY transceiver terminations see the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) or *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)).
9. For soldering guidelines and thermal considerations, see the *UltraScale and UltraScale+ FPGAs Packaging and Pinout Specifications* ([UG575](#)).

Table 2: Recommended Operating Conditions⁽¹⁾⁽²⁾

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
V _{CCINT}	Internal supply voltage.	0.825	0.850	0.876	V
	For -1LI and -2LE (0.72V only) devices: Internal supply voltage.	0.698	0.720	0.742	V
	For -3E devices: Internal supply voltage.	0.873	0.900	0.927	V
V _{CCINT_IO} ⁽³⁾	Internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -1LI and -2LE devices (0.85V only): internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -3E devices: internal supply voltage for the I/O banks.	0.873	0.900	0.927	V
V _{CCBRAM}	Block RAM supply voltage.	0.825	0.850	0.876	V
	For -3E devices: block RAM supply voltage.	0.873	0.900	0.927	V
V _{CCAUX}	Auxiliary supply voltage.	1.746	1.800	1.854	V
V _{CCO} ⁽⁴⁾⁽⁵⁾	Supply voltage for HD I/O banks.	1.140	–	3.400	V
	Supply voltage for HP I/O banks.	0.950	–	1.900	V
V _{CCAUX_IO} ⁽⁶⁾	Auxiliary I/O supply voltage.	1.746	1.800	1.854	V
V _{IN} ⁽⁷⁾	I/O input voltage.	–0.200	–	V _{CCO} + 0.200	V
I _{IN} ⁽⁸⁾	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–		mA
V _{BATT} ⁽⁹⁾	Battery voltage	1.000	–	1.890	V
GTH or GTY Transceiver					
V _{MGTAVCC} ⁽¹⁰⁾	Analog supply voltage for the GTH or GTY transceiver.	0.873	0.900	0.927	V
V _{MGTAVTT} ⁽¹⁰⁾	Analog supply voltage for the GTH or GTY transmitter and receiver termination circuits.	1.164	1.20	1.236	V
V _{MGTVCCAUX} ⁽¹⁰⁾	Auxiliary analog QPLL voltage supply for the transceivers.	1.746	1.80	1.854	V
V _{MGTAVTTRCAL} ⁽¹⁰⁾	Analog supply voltage for the resistor calibration circuit of the GTH or GTY transceiver column.	1.164	1.20	1.236	V

Table 2: Recommended Operating Conditions⁽¹⁾⁽²⁾ (Cont'd)

Symbol	Description	Min	Typ	Max	Units
SYSMON					
V _{CCADC}	SYSMON supply relative to GNDADC.	1.746	1.800	1.854	V
V _{REFP}	Externally supplied reference voltage.	1.200	1.250	1.300	V
Temperature					
T _j	Junction temperature operating range for extended (E) temperature devices. ⁽¹¹⁾	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices.	–40	–	100	°C

Notes:

- All voltages are relative to GND.
- For the design of the power distribution system consult *UltraScale Architecture PCB Design Guide* ([UG583](#)).
- V_{CCINT_IO} must be connected to V_{CCBRAM}.
- For V_{CCO_0}, the minimum recommended operating voltage for power on and during configuration is 1.425V. After configuration, data is retained even if V_{CCO} drops to 0V.
- Includes V_{CCO} of 1.0V (HP I/O only), 1.2V, 1.35V, 1.5V, 1.8V, 2.5V (HD I/O only) at ±5%, and 3.3V (HD I/O only) at +3/–5%.
- V_{CCAUX_IO} must be connected to V_{CCAUX}.
- The lower absolute voltage specification always applies.
- A total of 200 mA per 52-pin bank should not be exceeded.
- If battery is not used, connect V_{BATT} to either GND or V_{CCAUX}.
- Each voltage listed requires filtering as described in *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) or *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)).
- Devices labeled with the speed/temperature grade of -2LE can operate for a limited time at a junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage (nominal voltage of 0.85V or a low-voltage of 0.72V). Operation at T_j = 110°C is limited to 1% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 1% of the device lifetime.

Table 3: DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Min	Typ ⁽¹⁾	Max	Units
V _{DRINT}	Data retention V _{CCINT} voltage (below which configuration data might be lost).		–	–	V
V _{DRAUX}	Data retention V _{CCAUX} voltage (below which configuration data might be lost).		–	–	V
I _{REF}	V _{REF} leakage current per pin.	–	–		μA
I _L	Input or output leakage current per pin (sample-tested). ⁽²⁾	–	–		μA
C _{IN} ⁽³⁾	Die input capacitance at the pad (HP I/O).	–	–		pF
	Die input capacitance at the pad (HD I/O).	–	–		pF
I _{RPU}	Pad pull-up (when selected) at V _{IN} = 0V, V _{CCO} = 3.3V.		–		μA
	Pad pull-up (when selected) at V _{IN} = 0V, V _{CCO} = 2.5V.		–		μA
	Pad pull-up (when selected) at V _{IN} = 0V, V _{CCO} = 1.8V.		–		μA
	Pad pull-up (when selected) at V _{IN} = 0V, V _{CCO} = 1.5V.		–		μA
	Pad pull-up (when selected) at V _{IN} = 0V, V _{CCO} = 1.2V.		–		μA
I _{RPD}	Pad pull-down (when selected) at V _{IN} = 3.3V.		–		μA
	Pad pull-down (when selected) at V _{IN} = 1.8V.		–		μA
I _{CCADCON}	Analog supply current, analog circuits in power-up state.	–	–		mA
I _{CCADCOFF}	Analog supply current, analog circuits in power-down state.		–	–	mA
I _{BATT} ⁽⁴⁾⁽⁵⁾	Battery supply current.	150	–	250	nA
<i>Calibrated programmable on-die termination (DCI) in HP I/O banks⁽⁷⁾ (measured per JEDEC specification)</i>					
R ⁽⁸⁾	Thevenin equivalent resistance of programmable input termination to V _{CCO} /2 where ODT = RTT_40. ⁽⁶⁾		40		Ω
	Thevenin equivalent resistance of programmable input termination to V _{CCO} /2 where ODT = RTT_48. ⁽⁶⁾		48		Ω
	Thevenin equivalent resistance of programmable input termination to V _{CCO} /2 where ODT = RTT_60. ⁽⁶⁾		60		Ω
	Programmable input termination to V _{CCO} where ODT = RTT_40. ⁽⁶⁾		40		Ω
	Programmable input termination to V _{CCO} where ODT = RTT_48. ⁽⁶⁾		48		Ω
	Programmable input termination to V _{CCO} where ODT = RTT_60. ⁽⁶⁾		60		Ω
	Programmable input termination to V _{CCO} where ODT = RTT_120. ⁽⁶⁾		120		Ω
	Programmable input termination to V _{CCO} where ODT = RTT_240. ⁽⁶⁾		240		Ω

Table 3: DC Characteristics Over Recommended Operating Conditions (Cont'd)

Symbol	Description	Min	Typ ⁽¹⁾	Max	Units
<i>Uncalibrated programmable on-die termination in HP I/O banks (measured per JEDEC specification)</i>					
R ⁽⁸⁾	Thevenin equivalent resistance of programmable input termination to V _{CC0} /2 where ODT = RTT_40.		40		Ω
	Thevenin equivalent resistance of programmable input termination to V _{CC0} /2 where ODT = RTT_48.		48		Ω
	Thevenin equivalent resistance of programmable input termination to V _{CC0} /2 where ODT = RTT_60.		60		Ω
	Programmable input termination to V _{CC0} where ODT = RTT_40.		40		Ω
	Programmable input termination to V _{CC0} where ODT = RTT_48.		48		Ω
	Programmable input termination to V _{CC0} where ODT = RTT_60.		60		Ω
	Programmable input termination to V _{CC0} where ODT = RTT_120.		120		Ω
	Programmable input termination to V _{CC0} where ODT = RTT_240.		240		Ω
<i>Uncalibrated programmable on-die termination in HD I/O banks (measured per JEDEC specification)</i>					
R ⁽⁸⁾	Thevenin equivalent resistance of programmable input termination to V _{CC0} /2 where ODT = RTT_48.		48		Ω
Internal V _{REF}	50% V _{CC0}	V _{CC0} × 0.49	V _{CC0} × 0.50	V _{CC0} × 0.51	V
	70% V _{CC0}	V _{CC0} × 0.69	V _{CC0} × 0.70	V _{CC0} × 0.71	V
Differential termination	Programmable differential termination (TERM_100) for HP I/O banks.	–	100	–	Ω
n	Temperature diode ideality factor.	–	1.026	–	–
r	Temperature diode series resistance.	–		–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. For HP I/O banks with a V_{CC0} of 1.8V and separated V_{CC0} and V_{CCAUX_IO} power supplies, the I_L maximum current is 70 μA.
3. This measurement represents the die capacitance at the pad, not including the package.
4. Maximum value specified for worst case process at 25°C.
5. I_{BATT} is measured when the battery-backed RAM (BBRAM) is enabled.
6. If VRP resides at a different bank (DCI cascade), the range increases to ±15%.
7. VRP resistor tolerance is (240Ω ±1%)
8. On-die input termination resistance, for more information see the *UltraScale Architecture SelectIO Resources User Guide (UG571)*.

Table 4: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HD I/O Banks⁽¹⁾

AC Voltage Overshoot	% of UI at -40°C to 100°C	AC Voltage Undershoot	% of UI at -40°C to 100°C
$V_{CCO} + 0.30$			
$V_{CCO} + 0.35$			
$V_{CCO} + 0.40$			
$V_{CCO} + 0.45$			
$V_{CCO} + 0.50$			
$V_{CCO} + 0.55$			
$V_{CCO} + 0.60$			
$V_{CCO} + 0.65$			
$V_{CCO} + 0.70$			
$V_{CCO} + 0.75$			
$V_{CCO} + 0.80$			
$V_{CCO} + 0.85$			
$V_{CCO} + 0.90$			
$V_{CCO} + 0.95$			

Notes:

1. A total of 200 mA per bank should not be exceeded.

Table 5: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HP I/O Banks⁽¹⁾⁽²⁾

AC Voltage Overshoot	% of UI at -40°C to 100°C	AC Voltage Undershoot	% of UI at -40°C to 100°C
$V_{CCO} + 0.05$			
$V_{CCO} + 0.10$			
$V_{CCO} + 0.15$			
$V_{CCO} + 0.20$			
$V_{CCO} + 0.25$			
$V_{CCO} + 0.30$			
$V_{CCO} + 0.35$			
$V_{CCO} + 0.40$			
$V_{CCO} + 0.45$			
$V_{CCO} + 0.50$			
$V_{CCO} + 0.55$			
$V_{CCO} + 0.60$			
$V_{CCO} + 0.65$			
$V_{CCO} + 0.70$			
$V_{CCO} + 0.75$			
$V_{CCO} + 0.80$			
$V_{CCO} + 0.85$			

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 μs .

Table 6: Typical Quiescent Supply Current⁽¹⁾⁽²⁾⁽³⁾

Symbol	Description	Device	Speed Grade and V _{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
I _{CCINTQ}	Quiescent V _{CCINT} supply current.	XCKU3P						mA
		XCKU5P						mA
		XCKU9P	1690	1607	1607	1409	1409	mA
		XCKU11P						mA
		XCKU13P						mA
		XCKU15P						mA
I _{CCINT_IOQ}	Quiescent current for V _{CCINT_IO} supply.	XCKU3P						mA
		XCKU5P						mA
		XCKU9P	61	59	59	59	59	mA
		XCKU11P						mA
		XCKU13P						mA
		XCKU15P						mA
I _{CCOQ}	Quiescent V _{CCO} supply current.	XCKU3P						mA
		XCKU5P						mA
		XCKU9P	1	1	1	1	1	mA
		XCKU11P						mA
		XCKU13P						mA
		XCKU15P						mA
I _{CCAUXQ}	Quiescent V _{CCAUX} supply current.	XCKU3P						mA
		XCKU5P						mA
		XCKU9P	273	273	273	273	273	mA
		XCKU11P						mA
		XCKU13P						mA
		XCKU15P						mA
I _{CCAUX_IOQ}	Quiescent V _{CCAUX_IO} supply current.	XCKU3P						mA
		XCKU5P						mA
		XCKU9P	33	33	33	33	33	mA
		XCKU11P						mA
		XCKU13P						mA
		XCKU15P						mA

Table 6: Typical Quiescent Supply Current⁽¹⁾⁽²⁾⁽³⁾ (Cont'd)

Symbol	Description	Device	Speed Grade and V _{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
I _{CCBRAMQ}	Quiescent V _{CCBRAM} supply current.	XCKU3P						mA
		XCKU5P						mA
		XCKU9P	48	45	45	45	45	mA
		XCKU11P						mA
		XCKU13P						mA
		XCKU15P						mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCINT_IO}/V_{CCBRAM}, V_{CCAUX}/V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCINT_IO}/V_{CCBRAM} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCINT_IO} must be connected to V_{CCBRAM}. If V_{CCAUX}/V_{CCAUX_IO} and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCAUX} and V_{CCAUX_IO} must be connected together. V_{CCADC} and V_{REF} can be powered at any time and have no power-up sequencing requirements.

The recommended power-on sequence to achieve minimum current draw for the GTH or GTY transceivers is V_{CCINT}, V_{MGTAVCC}, V_{MGTAVTT} OR V_{MGTAVCC}, V_{CCINT}, V_{MGTAVTT}. There is no recommended sequencing for V_{MGTVCCAUX}. Both V_{MGTAVCC} and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from V_{MGTAVTT} can be higher than specifications during power-up and power-down.

Power Supply Requirements

Table 7 shows the minimum current, in addition to I_{CCQ} , that are required by the Kintex UltraScale+ FPGAs for proper power-on and configuration. If the current minimums shown in Table 6 and Table 7 are met, the device powers on after all supplies have passed through their power-on reset threshold voltages. The device must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) tools to estimate current drain on these supplies.

Table 7: Power-on Current by Device

Device	$I_{CCINTMIN}$	$I_{CCINT_IOMIN} + I_{CCBRAMMIN}$	I_{CCOMIN}	$I_{CCAUXMIN} + I_{CCAUX_IOMIN}$	Units
XCKU3P	$I_{CCINTQ} + 770$	$I_{CCBRAMQ} + I_{CCINT_IOQ} + 229$	$I_{CCOQ} + 50$	$I_{CCAUXQ} + I_{CCAUX_IOQ} + 386$	mA
XCKU5P	$I_{CCINTQ} + 770$	$I_{CCBRAMQ} + I_{CCINT_IOQ} + 305$	$I_{CCOQ} + 50$	$I_{CCAUXQ} + I_{CCAUX_IOQ} + 515$	mA
XCKU9P	$I_{CCINTQ} + 1800$	$I_{CCBRAMQ} + I_{CCINT_IOQ} + 600$	$I_{CCOQ} + 50$	$I_{CCAUXQ} + I_{CCAUX_IOQ} + 650$	mA
XCKU11P	$I_{CCINTQ} + 1961$	$I_{CCBRAMQ} + I_{CCINT_IOQ} + 654$	$I_{CCOQ} + 55$	$I_{CCAUXQ} + I_{CCAUX_IOQ} + 709$	mA
XCKU13P	$I_{CCINTQ} + 2242$	$I_{CCBRAMQ} + I_{CCINT_IOQ} + 748$	$I_{CCOQ} + 63$	$I_{CCAUXQ} + I_{CCAUX_IOQ} + 810$	mA
XCKU15P	$I_{CCINTQ} + 3433$	$I_{CCBRAMQ} + I_{CCINT_IOQ} + 1145$	$I_{CCOQ} + 96$	$I_{CCAUXQ} + I_{CCAUX_IOQ} + 1240$	mA

Table 8 shows the power supply ramp time.

Table 8: Power Supply Ramp Time

Symbol	Description	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 95% of V_{CCINT} .	0.2	40	ms
T_{VCCINT_IO}	Ramp time from GND to 95% of V_{CCINT_IO} .	0.2	40	ms
T_{VCCO}	Ramp time from GND to 95% of V_{CCO} .	0.2	40	ms
T_{VCCAUX}	Ramp time from GND to 95% of V_{CCAUX} .	0.2	40	ms
$T_{VCCBRAM}$	Ramp time from GND to 95% of V_{CCBRAM} .	0.2	40	ms
$T_{MGTAVCC}$	Ramp time from GND to 95% of $V_{MGTAVCC}$.	0.2	40	ms
$T_{MGTAVTT}$	Ramp time from GND to 95% of $V_{MGTAVTT}$.	0.2	40	ms
$T_{MGTVCCAUX}$	Ramp time from GND to 95% of $V_{MGTVCCAUX}$.	0.2	40	ms

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 9: SelectIO DC Input and Output Levels For HD I/O Banks⁽¹⁾⁽²⁾⁽³⁾

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	8.0	-8.0
HSTL_I_18	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	8.0	-8.0
HSUL_12	-0.300	$V_{REF} - 0.130$	$V_{REF} + 0.130$	$V_{CCO} + 0.300$	20% V_{CCO}	80% V_{CCO}	0.1	-0.1
LVC MOS12	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 4	Note 4
LVC MOS15	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.450	$V_{CCO} - 0.450$	Note 5	Note 5
LVC MOS18	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.450	$V_{CCO} - 0.450$	Note 5	Note 5
LVC MOS25	-0.300	0.700	1.700	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 5	Note 5
LVC MOS33	-0.300	0.800	2.000	3.400	0.400	$V_{CCO} - 0.400$	Note 5	Note 5
LV TTL	-0.300	0.800	2.000	3.400	0.400	2.400	Note 5	Note 5
SSTL12	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	14.25	-14.25
SSTL135	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	8.9	-8.9
SSTL135_II	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	13.0	-13.0
SSTL15	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.175$	$V_{CCO}/2 + 0.175$	8.9	-8.9
SSTL15_II	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.175$	$V_{CCO}/2 + 0.175$	13.0	-13.0
SSTL18_I	-0.300	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.470$	$V_{CCO}/2 + 0.470$	8.0	-8.0
SSTL18_II	-0.300	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.600$	$V_{CCO}/2 + 0.600$	13.4	-13.4
MIPI_DPHY_DCI_LP ⁽⁶⁾	-0.300	0.550	0.880	$V_{CCO} + 0.300$	0.050	1.100	0.01	-0.01

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. POD10 and POD12 DC input and output levels are shown in Table 11, Table 15, Table 16, and Table 17.
4. Supported drive strengths of 4, 8, or 12 mA in HD I/O banks.
5. Supported drive strengths of 4, 8, 12, or 16 mA in HD I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

Table 10: SelectIO DC Input and Output Levels for HP I/O Banks⁽¹⁾⁽²⁾⁽³⁾

I/O Standard	V _{IL}		V _{IH}		V _{OL}	V _{OH}	I _{OL}	I _{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	-0.300	V _{REF} - 0.100	V _{REF} + 0.100	V _{CCO} + 0.300	0.400	V _{CCO} - 0.400	5.8	-5.8
HSTL_I_12	-0.300	V _{REF} - 0.080	V _{REF} + 0.080	V _{CCO} + 0.300	25% V _{CCO}	75% V _{CCO}	4.1	-4.1
HSTL_I_18	-0.300	V _{REF} - 0.100	V _{REF} + 0.100	V _{CCO} + 0.300	0.400	V _{CCO} - 0.400	6.2	-6.2
HSUL_12	-0.300	V _{REF} - 0.130	V _{REF} + 0.130	V _{CCO} + 0.300	20% V _{CCO}	80% V _{CCO}	0.1	-0.1
LVC MOS12	-0.300	35% V _{CCO}	65% V _{CCO}	V _{CCO} + 0.300	0.400	V _{CCO} - 0.400	Note 4	Note 4
LVC MOS15	-0.300	35% V _{CCO}	65% V _{CCO}	V _{CCO} + 0.300	0.450	V _{CCO} - 0.450	Note 5	Note 5
LVC MOS18	-0.300	35% V _{CCO}	65% V _{CCO}	V _{CCO} + 0.300	0.450	V _{CCO} - 0.450	Note 5	Note 5
LVDCI_15	-0.300	35% V _{CCO}	65% V _{CCO}	V _{CCO} + 0.300	0.450	V _{CCO} - 0.450	7.0	-7.0
LVDCI_18	-0.300	35% V _{CCO}	65% V _{CCO}	V _{CCO} + 0.300	0.450	V _{CCO} - 0.450	7.0	-7.0
SSTL12	-0.300	V _{REF} - 0.100	V _{REF} + 0.100	V _{CCO} + 0.300	V _{CCO} /2 - 0.150	V _{CCO} /2 + 0.150	8.0	-8.0
SSTL135	-0.300	V _{REF} - 0.090	V _{REF} + 0.090	V _{CCO} + 0.300	V _{CCO} /2 - 0.150	V _{CCO} /2 + 0.150	9.0	-9.0
SSTL15	-0.300	V _{REF} - 0.100	V _{REF} + 0.100	V _{CCO} + 0.300	V _{CCO} /2 - 0.175	V _{CCO} /2 + 0.175	10.0	-10.0
SSTL18_I	-0.300	V _{REF} - 0.125	V _{REF} + 0.125	V _{CCO} + 0.300	V _{CCO} /2 - 0.470	V _{CCO} /2 + 0.470	7.0	-7.0
MIPI_DPHY_DCI_LP ⁽⁶⁾	-0.300	0.550	0.880	V _{CCO} + 0.300	0.050	1.100	0.01	-0.01

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).
3. POD10 and POD12 DC input and output levels are shown in [Table 11](#), [Table 15](#), [Table 16](#), and [Table 17](#).
4. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in HP I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

Table 11: DC Input Levels for Single-ended POD10 and POD12 I/O Standards⁽¹⁾⁽²⁾

I/O Standard	V _{IL}		V _{IH}	
	V, Min	V, Max	V, Min	V, Max
POD10	-0.300	V _{REF} - 0.068	V _{REF} + 0.068	V _{CCO} + 0.300
POD12	-0.300	V _{REF} - 0.068	V _{REF} + 0.068	V _{CCO} + 0.300

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).

Table 12: Differential SelectIO DC Input and Output Levels

I/O Standard	V _{ICM} (V) (1)			V _{ID} (V) (2)			V _{ILHS} (3)	V _{IHHS} (3)	V _{Ocm} (V) (4)			V _{OD} (V) (5)		
	Min	Typ	Max	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
SUB_LVDS(8)	0.500	0.900	1.300	0.070	–	–	–	–	0.700	0.900	1.100	0.100	0.150	0.200
LVPECL	0.300	1.200	1.425	0.100	0.350	0.600	–	–	–	–	–	–	–	–
SLVS_400_18	0.070	0.200	0.330	0.140	–	0.450	–	–	–	–	–	–	–	–
SLVS_400_25	0.070	0.200	0.330	0.140	–	0.450	–	–	–	–	–	–	–	–
MIPI_DPHY_DCI_HS(9)	0.070		0.330	0.070	–	–	–0.040	0.460	0.150	0.200	0.250	0.140	0.200	0.270

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – Q̄).
3. V_{IHHS} and V_{ILHS} are the single-ended input high and low voltages, respectively.
4. V_{Ocm} is the output common mode voltage.
5. V_{OD} is the output differential voltage (Q – Q̄).
6. LVDS_25 is specified in Table 18.
7. LVDS is specified in Table 19.
8. Only the SUB_LVDS receiver is supported in HD I/O banks.
9. High-speed option for MIPI_DPHY_DCI. The V_{ID} maximum is aligned with the standard's specification. A higher V_{ID} is acceptable as long as the V_{IN} specification is also met.

Table 13: Complementary Differential SelectIO DC Input and Output Levels for HD I/O Banks

I/O Standard	V _{ICM} (V) (1)			V _{ID} (V) (2)		V _{OL} (V) (3)	V _{OH} (V) (4)	I _{OL}	I _{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V _{CCO} – 0.400	8.0	–8.0
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V _{CCO} – 0.400	8.0	–8.0
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V _{CCO}	80% V _{CCO}	0.1	–0.1
DIFF_SSTL12	0.300	0.600	0.850	0.100	–	(V _{CCO} /2) – 0.150	(V _{CCO} /2) + 0.150	14.25	–14.25
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V _{CCO} /2) – 0.150	(V _{CCO} /2) + 0.150	8.9	–8.9
DIFF_SSTL135_II	0.300	0.675	1.000	0.100	–	(V _{CCO} /2) – 0.150	(V _{CCO} /2) + 0.150	13.0	–13.0
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V _{CCO} /2) – 0.175	(V _{CCO} /2) + 0.175	8.9	–8.9
DIFF_SSTL15_II	0.300	0.750	1.125	0.100	–	(V _{CCO} /2) – 0.175	(V _{CCO} /2) + 0.175	13.0	–13.0
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V _{CCO} /2) – 0.470	(V _{CCO} /2) + 0.470	8.0	–8.0
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	(V _{CCO} /2) – 0.600	(V _{CCO} /2) + 0.600	13.4	–13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage.
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

Table 14: Complementary Differential SelectIO DC Input and Output Levels for HP I/O Banks⁽¹⁾

I/O Standard	V_{ICM} (V) ⁽²⁾			V_{ID} (V) ⁽³⁾		V_{OL} (V) ⁽⁴⁾	V_{OH} (V) ⁽⁵⁾	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.680	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	0.400	$V_{CCO} - 0.400$	5.8	–5.8
DIFF_HSTL_I_12	$0.400 \times V_{CCO}$	$V_{CCO}/2$	$0.600 \times V_{CCO}$	0.100	–	$0.250 \times V_{CCO}$	$0.750 \times V_{CCO}$	4.1	–4.1
DIFF_HSTL_I_18	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	0.400	$V_{CCO} - 0.400$	6.2	–6.2
DIFF_HSUL_12	$(V_{CCO}/2) - 0.120$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.120$	0.100	–	$20\% V_{CCO}$	$80\% V_{CCO}$	0.1	–0.1
DIFF_SSTL12	$(V_{CCO}/2) - 0.150$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	8.0	–8.0
DIFF_SSTL135	$(V_{CCO}/2) - 0.150$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	9.0	–9.0
DIFF_SSTL15	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	10.0	–10.0
DIFF_SSTL18_I	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	$(V_{CCO}/2) - 0.470$	$(V_{CCO}/2) + 0.470$	7.0	–7.0

Notes:

1. DIFF_POD10 and DIFF_POD12 HP I/O bank specifications are shown in [Table 15](#), [Table 16](#), and [Table 17](#).
2. V_{ICM} is the input common mode voltage.
3. V_{ID} is the input differential voltage.
4. V_{OL} is the single-ended low-output voltage.
5. V_{OH} is the single-ended high-output voltage.

Table 15: DC Input Levels for Differential POD10 and POD12 I/O Standards⁽¹⁾⁽²⁾

I/O Standard	V_{ICM} (V)			V_{ID} (V)	
	Min	Typ	Max	Min	Max
DIFF_POD10	0.63	0.70	0.77	0.14	–
DIFF_POD12	0.76	0.84	0.92	0.16	–

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).

Table 16: DC Output Levels for Single-ended and Differential POD10 and POD12 Standards⁽¹⁾⁽²⁾

Symbol	Description	V_{OUT}	Min	Typ	Max	Units
R_{OL}	Pull-down resistance.	V_{OM_DC} (as described in Table 17)	36	40	44	Ω
R_{OH}	Pull-up resistance.	V_{OM_DC} (as described in Table 17)	36	40	44	Ω

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).

Table 17: [Table 16](#) Definitions for DC Output Levels for POD Standards

Symbol	Description	All Speed Grades	Units
V_{OM_DC}	DC output Mid measurement level (for IV curve linearity).	$0.8 \times V_{CCO}$	V

LVDS DC Specifications (LVDS_25)

The LVDS_25 standard is available in the HD I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)) for more information.

Table 18: LVDS_25 DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
$V_{CCO}^{(1)}$	Supply voltage.		2.375	2.500	2.625	V
V_{IDIFF}	Differential input voltage: ($\overline{Q} - Q$), $\overline{Q} = \text{High}$ ($Q - \overline{Q}$), $Q = \text{High}$		100	350	600 ⁽²⁾	mV
V_{ICM}	Input common-mode voltage.		0.300	1.200	1.500	V

Notes:

1. HD I/O banks only support LVDS_25 inputs. LVDS_25 inputs without internal termination have no V_{CCO} requirements. Any V_{CCO} can be chosen as long as the input voltage levels do not violate the *Recommended Operating Condition* (Table 2) specification for the V_{IN} I/O pin voltage.
2. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM} , a higher V_{IDIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)) for more information.

Table 19: LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
$V_{CCO}^{(1)}$	Supply voltage.		1.710	1.800	1.890	V
$V_{ODIFF}^{(2)}$	Differential output voltage: ($\overline{Q} - Q$), $\overline{Q} = \text{High}$ ($Q - \overline{Q}$), $Q = \text{High}$	$R_T = 100\Omega$ across Q and \overline{Q} signals	247	350	600	mV
$V_{OCM}^{(2)}$	Output common-mode voltage.	$R_T = 100\Omega$ across Q and \overline{Q} signals	1.000	1.250	1.425	V
$V_{IDIFF}^{(3)}$	Differential input voltage: ($\overline{Q} - Q$), $\overline{Q} = \text{High}$ ($Q - \overline{Q}$), $Q = \text{High}$		100	350	600 ⁽³⁾	mV
$V_{ICM_DC}^{(4)}$	Input common-mode voltage (DC coupling).		0.300	1.200	1.425	V
$V_{ICM_AC}^{(5)}$	Input common-mode voltage (AC coupling).		0.600	–	1.100	V

Notes:

1. In HP I/O banks, when LVDS is used with input-only functionality, it can be placed in a bank where the V_{CCO} levels are different from the specified level only if internal differential termination is not used. In this scenario, V_{CCO} must be chosen to ensure the input pin voltage levels do not violate the *Recommended Operating Condition* (Table 2) specification for the V_{IN} I/O pin voltage.
2. V_{OCM} and V_{ODIFF} values are for $LVDS_PRE_EMPHASIS = \text{FALSE}$.
3. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM} , a higher V_{IDIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.
4. Input common mode voltage for DC coupled configurations. $EQUALIZATION = \text{EQ_NONE}$ (Default).
5. External input common mode voltage specification for AC coupled configurations. $EQUALIZATION = \text{EQ_LEVEL0}$, EQ_LEVEL1 , EQ_LEVEL2 , EQ_LEVEL3 , EQ_LEVEL4 .

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite as outlined in [Table 20](#).

Table 20: Speed Specification Version By Device

2016.1	Device
1.04	XCKU3P, XCKU5P, XCKU9P, XCKU11P, XCKU13P, and XCKU15P

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Kintex UltraScale+ FPGAs.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. [Table 21](#) correlates the current status of the Kintex UltraScale+ FPGAs on a per speed grade basis.

Table 21: Speed Grade Designations by Device

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	Preliminary	Production
XCKU3P	-3E ($V_{CCINT} = 0.90V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$), -1LI ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$), -1LI ($V_{CCINT} = 0.72V$)		
XCKU5P	-3E ($V_{CCINT} = 0.90V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$), -1LI ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$), -1LI ($V_{CCINT} = 0.72V$)		
XCKU9P	-3E ($V_{CCINT} = 0.90V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$), -1LI ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$), -1LI ($V_{CCINT} = 0.72V$)		
XCKU11P	-3E ($V_{CCINT} = 0.90V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$), -1LI ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$), -1LI ($V_{CCINT} = 0.72V$)		
XCKU13P	-3E ($V_{CCINT} = 0.90V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$), -1LI ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$), -1LI ($V_{CCINT} = 0.72V$)		
XCKU15P	-3E ($V_{CCINT} = 0.90V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$), -1LI ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$), -1LI ($V_{CCINT} = 0.72V$)		

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 22 lists the production released Kintex UltraScale+ FPGAs, speed grade, and the minimum corresponding supported speed specification version and Vivado software revisions. The Vivado software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 22: Kintex UltraScale+ FPGA Device Production Software and Speed Specification Release

Device	Speed Grade and V _{CCINT} Operating Voltages				
	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	-1
XCKU3P					
XCKU5P					
XCKU9P					
XCKU11P					
XCKU13P					
XCKU15P					

Notes:

- Blank entries indicate a device and/or speed grade in Advance or Preliminary status.

FPGA Logic Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Kintex UltraScale+ FPGAs. These values are subject to the same guidelines as the [AC Switching Characteristics, page 17](#). In each table, the I/O bank type is either high performance (HP) or high density (HD).

Table 23: LVDS Component Mode Performance

Description	I/O Bank Type	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
LVDS TX DDR (OSERDES 4:1, 8:1)	HP	1250	1250	1250	1250	1250	Mb/s
LVDS TX SDR (OSERDES 2:1, 4:1)	HP	710	710	625	710	625	Mb/s
LVDS RX DDR (ISERDES 1:4, 1:8) ⁽¹⁾	HP	1250	1250	1250	1250	1250	Mb/s
	HD						Mb/s
LVDS RX SDR (ISERDES 1:2, 1:4) ⁽¹⁾	HP	710	710	625	710	625	Mb/s
	HD						Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) or phase-tracking algorithms are used to achieve maximum performance.

Table 24: LVDS Native Mode Performance⁽¹⁾

Description	I/O Bank Type	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
LVDS TX DDR (TX_BITSLICE 4:1, 8:1)	HP	1600	1600	1250	1600	1250	Mb/s
LVDS TX SDR (TX_BITSLICE 2:1, 4:1)	HP	800	800	625	800	625	Mb/s
LVDS RX DDR (RX_BITSLICE 1:4, 1:8) ⁽²⁾	HP	1600	1600	1250	1600	1250	Mb/s
LVDS RX SDR (RX_BITSLICE 1:2, 1:4) ⁽²⁾	HP	800	800	625	800	625	Mb/s

Notes:

1. Native mode is supported through the [High-Speed SelectIO Interface Wizard](#) available with the Vivado Design Suite.
2. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) or phase-tracking algorithms are used to achieve maximum performance.

Table 25: LVDS Native-Mode 1000BASE-X Support⁽¹⁾

Description	I/O Bank Type	Speed Grade and V _{CCINT} Operating Voltages				
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	-1
1000BASE-X	HP	Yes				

Notes:

1. 1000BASE-X support is based on the *IEEE Standard for CSMA/CD Access Method and Physical Layer Specifications* (IEEE Std 802.3-2008).

Table 26 provides the maximum data rates for applicable memory standards using the Kintex UltraScale+ FPGA memory PHY. Refer to [Memory Interfaces](#) for the complete list of memory interface standards supported and detailed specifications. The final performance of the memory interface is determined through a complete design implemented in the Vivado Design Suite, following guidelines in the *UltraScale Architecture PCB Design Guide (UG583)*, electrical analysis, and characterization of the system.

Table 26: Maximum Physical Interface (PHY) Rate for Memory Interfaces

Memory Standard	Package	DRAM Type	Speed Grade and V _{CCINT} Operating Voltages					Units	
			0.90V		0.85V		0.72V		
			-3	-2	-1	-2	-1		
DDR4	All FFV packages	Single rank component	2666	2666	2400	2400	2133	Mb/s	
		1 rank DIMM ⁽¹⁾⁽²⁾	2400	2400	2133	2133	1866	Mb/s	
		2 rank DIMM ⁽¹⁾⁽³⁾	2133	2133	1866	1866	1600	Mb/s	
		4 rank DIMM ⁽¹⁾⁽⁴⁾	1600	1600	1333	1333	N/A	Mb/s	
	SFVB784	Single rank component	2400	2400	2133	2133	1866	Mb/s	
		1 rank DIMM ⁽¹⁾⁽²⁾	2133	2133	1866	1866	1600	Mb/s	
DDR3	All FFV packages	Single rank component	2133	2133	2133	2133	1866	Mb/s	
		1 rank DIMM ⁽¹⁾⁽²⁾	1866	1866	1866	1866	1600	Mb/s	
		2 rank DIMM ⁽¹⁾⁽³⁾	1600	1600	1600	1600	1333	Mb/s	
		4 rank DIMM ⁽¹⁾⁽⁴⁾	1066	1066	1066	1066	800	Mb/s	
	SFVB784	Single rank component	1866	1866	1866	1866	1600	Mb/s	
		1 rank DIMM ⁽¹⁾⁽²⁾	1600	1600	1600	1600	1333	Mb/s	
		2 rank DIMM ⁽¹⁾⁽³⁾	1333	1333	1333	1333	1066	Mb/s	
		4 rank DIMM ⁽¹⁾⁽⁴⁾	800	800	800	800	606	Mb/s	
	DDR3L	All FFV packages	Single rank component	1866	1866	1866	1866	1600	Mb/s
			1 rank DIMM ⁽¹⁾⁽²⁾	1600	1600	1600	1600	1333	Mb/s
			2 rank DIMM ⁽¹⁾⁽³⁾	1333	1333	1333	1333	1066	Mb/s
			4 rank DIMM ⁽¹⁾⁽⁴⁾	800	800	800	800	606	Mb/s
SFVB784		Single rank component	1600	1600	1600	1600	1600	Mb/s	
		1 rank DIMM ⁽¹⁾⁽²⁾	1333	1333	1333	1333	1333	Mb/s	
		2 rank DIMM ⁽¹⁾⁽³⁾	1066	1066	1066	1066	1066	Mb/s	
		4 rank DIMM ⁽¹⁾⁽⁴⁾	606	606	606	606	606	Mb/s	
QDR II+	All	Single rank component ⁽⁵⁾	633	633	600	600	550	MHz	
RLDRAM 3	All FFV packages	Single rank component	1200	1200	1066	1066	933	MHz	
	SFVB784	Single rank component	1066	1066	933	933	800	MHz	
QDR IV XP	All	Single rank component ⁽⁶⁾	1066	1066	1066	933	933	MHz	
LPDDR3	All	Single rank component	1600	1600	1600	1600	1600	Mb/s	

Notes:

1. Dual in-line memory module (DIMM) includes RDIMM, SODIMM, UDIMM, and LRDIMM.
2. Includes: 1 rank 1 slot, DDP 2 rank, LRDIMM 2 or 4 rank 1 slot.
3. Includes: 2 rank 1 slot, 1 rank 2 slot, LRDIMM 2 rank 2 slot.
4. Includes: 2 rank 2 slot, 4 rank 1 slot.
5. The QDR II+ performance specifications are for burst-length 4 (BL = 4) implementations.
6. This memory interface is not production qualified and specification is subject to change.

IOB Pad Input, Output, and 3-State

Table 27 (high-density IOB (HD)) and Table 28 (high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{INBUF_DELAY_PAD_I}$ is the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{OUTBUF_DELAY_O_PAD}$ is the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{OUTBUF_DELAY_TD_PAD}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than $T_{OUTBUF_DELAY_TD_PAD}$ when the DCITERMDISABLE pin is used. In HD I/O banks, the on-die termination turn-on time is always faster than $T_{OUTBUF_DELAY_TD_PAD}$ when the INTERMDISABLE pin is used.

Table 27: IOB High Density (HD) Switching Characteristics

I/O Standards	$T_{INBUF_DELAY_PAD_I}$					$T_{OUTBUF_DELAY_O_PAD}$					$T_{OUTBUF_DELAY_TD_PAD}$					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
DIFF_HSTL_I_18_F	0.569	0.577	0.638	0.577	0.558	1.359	1.452	1.587	1.452	1.456	1.359	1.452	1.587	1.452	1.456	ns
DIFF_HSTL_I_18_S	0.569	0.577	0.638	0.577	0.558	1.359	1.452	1.587	1.452	1.456	1.359	1.452	1.587	1.452	1.456	ns
DIFF_HSTL_I_F	0.566	0.56	0.633	0.56	0.552	1.464	1.575	1.725	1.575	1.574	1.464	1.575	1.725	1.575	1.574	ns
DIFF_HSTL_I_S	0.566	0.56	0.633	0.56	0.552	1.464	1.575	1.725	1.575	1.574	1.464	1.575	1.725	1.575	1.574	ns
DIFF_HSUL_12_F	0.562	0.547	0.599	0.547	0.522	1.395	1.508	1.634	1.508	1.506	1.395	1.508	1.634	1.508	1.506	ns
DIFF_HSUL_12_S	0.562	0.547	0.599	0.547	0.522	1.395	1.508	1.634	1.508	1.506	1.395	1.508	1.634	1.508	1.506	ns
DIFF_SSTL12_F	0.566	0.552	0.609	0.552	0.522	1.463	1.561	1.704	1.561	1.555	1.463	1.561	1.704	1.561	1.555	ns
DIFF_SSTL12_S	0.566	0.552	0.609	0.552	0.522	1.707	1.747	1.909	1.747	1.716	1.707	1.747	1.909	1.747	1.716	ns
DIFF_SSTL135_F	0.577	0.560	0.613	0.56	0.527	1.473	1.590	1.728	1.590	1.585	1.473	1.590	1.728	1.590	1.585	ns
DIFF_SSTL135_II_F	0.577	0.560	0.613	0.56	0.527	1.406	1.498	1.636	1.498	1.491	1.406	1.498	1.636	1.498	1.491	ns
DIFF_SSTL135_II_S	0.577	0.560	0.613	0.56	0.527	1.576	1.649	1.789	1.649	1.618	1.576	1.649	1.789	1.649	1.618	ns
DIFF_SSTL135_S	0.577	0.560	0.613	0.56	0.527	1.817	1.887	2.046	1.887	1.846	1.817	1.887	2.046	1.887	1.846	ns
DIFF_SSTL15_F	0.566	0.560	0.633	0.56	0.552	1.474	1.592	1.734	1.592	1.597	1.474	1.592	1.734	1.592	1.597	ns
DIFF_SSTL15_II_F	0.566	0.560	0.633	0.56	0.552	1.406	1.511	1.659	1.511	1.505	1.406	1.511	1.659	1.511	1.505	ns
DIFF_SSTL15_II_S	0.566	0.560	0.633	0.56	0.552	1.618	1.700	1.856	1.700	1.668	1.618	1.700	1.856	1.700	1.668	ns
DIFF_SSTL15_S	0.566	0.560	0.633	0.56	0.552	1.734	1.804	1.957	1.804	1.775	1.734	1.804	1.957	1.804	1.775	ns
DIFF_SSTL18_II_F	0.569	0.577	0.638	0.577	0.558	1.357	1.473	1.604	1.473	1.469	1.357	1.473	1.604	1.473	1.469	ns
DIFF_SSTL18_II_S	0.569	0.577	0.638	0.577	0.558	1.511	1.629	1.784	1.629	1.616	1.511	1.629	1.784	1.629	1.616	ns
DIFF_SSTL18_I_F	0.569	0.577	0.638	0.577	0.558	1.335	1.431	1.563	1.431	1.429	1.335	1.431	1.563	1.431	1.429	ns
DIFF_SSTL18_I_S	0.569	0.577	0.638	0.577	0.558	1.692	1.802	1.961	1.802	1.760	1.692	1.802	1.961	1.802	1.760	ns
HSTL_I_18_F	0.596	0.606	0.668	0.606	0.571	1.359	1.452	1.587	1.452	1.456	1.359	1.452	1.587	1.452	1.456	ns
HSTL_I_18_S	0.596	0.606	0.668	0.606	0.571	1.359	1.452	1.587	1.452	1.456	1.359	1.452	1.587	1.452	1.456	ns
HSTL_I_F	0.597	0.601	0.604	0.601	0.566	1.464	1.575	1.725	1.575	1.574	1.464	1.575	1.725	1.575	1.574	ns
HSTL_I_S	0.597	0.601	0.604	0.601	0.566	1.464	1.575	1.725	1.575	1.574	1.464	1.575	1.725	1.575	1.574	ns
HSUL_12_F	0.604	0.598	0.615	0.598	0.538	1.395	1.508	1.634	1.508	1.506	1.395	1.508	1.634	1.508	1.506	ns
HSUL_12_S	0.604	0.598	0.615	0.598	0.538	1.395	1.508	1.634	1.508	1.506	1.395	1.508	1.634	1.508	1.506	ns

Table 27: IOB High Density (HD) Switching Characteristics (Cont'd)

I/O Standards	T _{INBUF_DELAY_PAD_I}					T _{OUTBUF_DELAY_O_PAD}					T _{OUTBUF_DELAY_TD_PAD}					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
LVC MOS12_F_12	0.515	0.558	0.618	0.558	0.568	1.465	1.574	1.733	1.574	1.566	1.465	1.574	1.733	1.574	1.566	ns
LVC MOS12_F_4	0.515	0.558	0.618	0.558	0.568	1.628	1.705	1.883	1.705	1.714	1.628	1.705	1.883	1.705	1.714	ns
LVC MOS12_F_8	0.515	0.558	0.618	0.558	0.568	1.480	1.540	1.690	1.540	1.533	1.480	1.540	1.690	1.540	1.533	ns
LVC MOS12_S_12	0.515	0.558	0.618	0.558	0.568	1.874	1.975	2.142	1.975	1.931	1.874	1.975	2.142	1.975	1.931	ns
LVC MOS12_S_4	0.515	0.558	0.618	0.558	0.568	1.935	1.959	2.162	1.959	1.949	1.935	1.959	2.162	1.959	1.949	ns
LVC MOS12_S_8	0.515	0.558	0.618	0.558	0.568	2.042	2.081	2.273	2.081	2.041	2.042	2.081	2.273	2.081	2.041	ns
LVC MOS15_F_12	0.468	0.513	0.588	0.513	0.530	1.374	1.422	1.573	1.422	1.439	1.374	1.422	1.573	1.422	1.439	ns
LVC MOS15_F_16	0.468	0.513	0.588	0.513	0.530	1.352	1.430	1.564	1.430	1.427	1.352	1.430	1.564	1.430	1.427	ns
LVC MOS15_F_4	0.468	0.513	0.588	0.513	0.530	1.539	1.626	1.747	1.626	1.636	1.539	1.626	1.747	1.626	1.636	ns
LVC MOS15_F_8	0.468	0.513	0.588	0.513	0.530	1.461	1.529	1.661	1.529	1.503	1.461	1.529	1.661	1.529	1.503	ns
LVC MOS15_S_12	0.468	0.513	0.588	0.513	0.530	1.778	1.859	1.999	1.859	1.823	1.778	1.859	1.999	1.859	1.823	ns
LVC MOS15_S_16	0.468	0.513	0.588	0.513	0.530	2.060	2.089	2.300	2.089	2.026	2.060	2.089	2.300	2.089	2.026	ns
LVC MOS15_S_4	0.468	0.513	0.588	0.513	0.530	2.160	2.204	2.368	2.204	2.115	2.160	2.204	2.368	2.204	2.115	ns
LVC MOS15_S_8	0.468	0.513	0.588	0.513	0.530	2.081	2.088	2.311	2.088	2.063	2.081	2.088	2.311	2.088	2.063	ns
LVC MOS18_F_12	0.437	0.502	0.512	0.502	0.497	1.393	1.487	1.618	1.487	1.460	1.393	1.487	1.618	1.487	1.460	ns
LVC MOS18_F_16	0.437	0.502	0.512	0.502	0.497	1.356	1.459	1.568	1.459	1.429	1.356	1.459	1.568	1.459	1.429	ns
LVC MOS18_F_4	0.437	0.502	0.512	0.502	0.497	1.572	1.650	1.780	1.650	1.634	1.572	1.650	1.780	1.650	1.634	ns
LVC MOS18_F_8	0.437	0.502	0.512	0.502	0.497	1.478	1.546	1.704	1.546	1.540	1.478	1.546	1.704	1.546	1.540	ns
LVC MOS18_S_12	0.437	0.502	0.512	0.502	0.497	1.993	2.038	2.232	2.038	1.999	1.993	2.038	2.232	2.038	1.999	ns
LVC MOS18_S_16	0.437	0.502	0.512	0.502	0.497	1.935	2.012	2.189	2.012	1.966	1.935	2.012	2.189	2.012	1.966	ns
LVC MOS18_S_4	0.437	0.502	0.512	0.502	0.497	2.123	2.154	2.358	2.154	2.100	2.123	2.154	2.358	2.154	2.100	ns
LVC MOS18_S_8	0.437	0.502	0.512	0.502	0.497	2.100	2.123	2.328	2.123	2.076	2.100	2.123	2.328	2.123	2.076	ns
LVC MOS25_F_12	0.516	0.542	0.588	0.542	0.539	1.961	2.012	2.296	2.012	2.001	1.961	2.012	2.296	2.012	2.001	ns
LVC MOS25_F_16	0.516	0.542	0.588	0.542	0.539	1.893	1.967	2.251	1.967	1.958	1.893	1.967	2.251	1.967	1.958	ns
LVC MOS25_F_4	0.516	0.542	0.588	0.542	0.539	2.100	2.213	2.413	2.213	2.155	2.100	2.213	2.413	2.213	2.155	ns
LVC MOS25_F_8	0.516	0.542	0.588	0.542	0.539	2.052	2.101	2.423	2.101	2.093	2.052	2.101	2.423	2.101	2.093	ns
LVC MOS25_S_12	0.516	0.542	0.588	0.542	0.539	2.455	2.589	2.878	2.589	2.501	2.455	2.589	2.878	2.589	2.501	ns
LVC MOS25_S_16	0.516	0.542	0.588	0.542	0.539	2.360	2.478	2.775	2.478	2.382	2.360	2.478	2.775	2.478	2.382	ns
LVC MOS25_S_4	0.516	0.542	0.588	0.542	0.539	2.622	2.723	3.016	2.723	2.630	2.622	2.723	3.016	2.723	2.630	ns
LVC MOS25_S_8	0.516	0.542	0.588	0.542	0.539	2.538	2.643	2.943	2.643	2.567	2.538	2.643	2.943	2.643	2.567	ns
LVC MOS33_F_12	0.577	0.622	0.675	0.622	0.624	1.942	2.047	2.248	2.047	2.024	1.942	2.047	2.248	2.047	2.024	ns
LVC MOS33_F_16	0.577	0.622	0.675	0.622	0.624	1.976	2.072	2.266	2.072	2.048	1.976	2.072	2.266	2.072	2.048	ns
LVC MOS33_F_4	0.577	0.622	0.675	0.622	0.624	1.925	2.049	2.232	2.049	2.019	1.925	2.049	2.232	2.049	2.019	ns
LVC MOS33_F_8	0.577	0.622	0.675	0.622	0.624	2.101	2.189	2.375	2.189	2.149	2.101	2.189	2.375	2.189	2.149	ns
LVC MOS33_S_12	0.577	0.622	0.675	0.622	0.624	2.450	2.533	2.856	2.533	2.515	2.450	2.533	2.856	2.533	2.515	ns
LVC MOS33_S_16	0.577	0.622	0.675	0.622	0.624	2.424	2.495	2.782	2.495	2.430	2.424	2.495	2.782	2.495	2.430	ns
LVC MOS33_S_4	0.577	0.622	0.675	0.622	0.624	2.632	2.684	2.991	2.684	2.613	2.632	2.684	2.991	2.684	2.613	ns
LVC MOS33_S_8	0.577	0.622	0.675	0.622	0.624	2.561	2.644	2.946	2.644	2.578	2.561	2.644	2.946	2.644	2.578	ns
LVDS_25	0.597	0.587	0.671	0.587	0.598	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVPECL	0.597	0.587	0.671	0.587	0.598	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVTTL_F_12	0.577	0.622	0.675	0.622	0.624	1.942	2.047	2.248	2.047	2.024	1.942	2.047	2.248	2.047	2.024	ns

Table 27: IOB High Density (HD) Switching Characteristics (Cont'd)

I/O Standards	T _{INBUF_DELAY_PAD_I}					T _{OUTBUF_DELAY_O_PAD}					T _{OUTBUF_DELAY_TD_PAD}					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
LVTTTL_F_16	0.577	0.622	0.675	0.622	0.624	1.994	2.144	2.379	2.144	2.081	1.994	2.144	2.379	2.144	2.081	ns
LVTTTL_F_4	0.577	0.622	0.675	0.622	0.624	1.925	2.049	2.232	2.049	2.019	1.925	2.049	2.232	2.049	2.019	ns
LVTTTL_F_8	0.577	0.622	0.675	0.622	0.624	2.093	2.190	2.365	2.190	2.144	2.093	2.190	2.365	2.190	2.144	ns
LVTTTL_S_12	0.577	0.622	0.675	0.622	0.624	2.450	2.533	2.856	2.533	2.515	2.450	2.533	2.856	2.533	2.515	ns
LVTTTL_S_16	0.577	0.622	0.675	0.622	0.624	2.424	2.495	2.782	2.495	2.430	2.424	2.495	2.782	2.495	2.430	ns
LVTTTL_S_4	0.577	0.622	0.675	0.622	0.624	2.632	2.684	2.991	2.684	2.613	2.632	2.684	2.991	2.684	2.613	ns
LVTTTL_S_8	0.577	0.622	0.675	0.622	0.624	2.561	2.644	2.946	2.644	2.578	2.561	2.644	2.946	2.644	2.578	ns
SLVS_400_25	0.597	0.587	0.671	0.587	0.598	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_F	0.604	0.598	0.615	0.598	0.538	1.463	1.561	1.704	1.561	1.555	1.463	1.561	1.704	1.561	1.555	ns
SSTL12_S	0.604	0.598	0.615	0.598	0.538	1.707	1.747	1.909	1.747	1.716	1.707	1.747	1.909	1.747	1.716	ns
SSTL135_F	0.605	0.598	0.642	0.598	0.552	1.473	1.590	1.728	1.59	1.585	1.473	1.590	1.728	1.590	1.585	ns
SSTL135_II_F	0.605	0.598	0.642	0.598	0.552	1.406	1.498	1.636	1.498	1.491	1.406	1.498	1.636	1.498	1.491	ns
SSTL135_II_S	0.605	0.598	0.642	0.598	0.552	1.576	1.649	1.789	1.649	1.618	1.576	1.649	1.789	1.649	1.618	ns
SSTL135_S	0.605	0.598	0.642	0.598	0.552	1.817	1.887	2.046	1.887	1.846	1.817	1.887	2.046	1.887	1.846	ns
SSTL15_F	0.597	0.601	0.604	0.601	0.566	1.474	1.592	1.734	1.592	1.597	1.474	1.592	1.734	1.592	1.597	ns
SSTL15_II_F	0.597	0.601	0.604	0.601	0.566	1.406	1.511	1.659	1.511	1.505	1.406	1.511	1.659	1.511	1.505	ns
SSTL15_II_S	0.597	0.601	0.604	0.601	0.566	1.618	1.700	1.856	1.700	1.668	1.618	1.700	1.856	1.700	1.668	ns
SSTL15_S	0.597	0.601	0.604	0.601	0.566	1.734	1.804	1.957	1.804	1.775	1.734	1.804	1.957	1.804	1.775	ns
SSTL18_II_F	0.596	0.606	0.668	0.606	0.571	1.357	1.473	1.604	1.473	1.469	1.357	1.473	1.604	1.473	1.469	ns
SSTL18_II_S	0.596	0.606	0.668	0.606	0.571	1.511	1.629	1.784	1.629	1.616	1.511	1.629	1.784	1.629	1.616	ns
SSTL18_I_F	0.596	0.606	0.668	0.606	0.571	1.335	1.431	1.563	1.431	1.429	1.335	1.431	1.563	1.431	1.429	ns
SSTL18_I_S	0.596	0.606	0.668	0.606	0.571	1.692	1.802	1.961	1.802	1.76	1.692	1.802	1.961	1.802	1.760	ns
SUB_LVDS	0.638	0.600	0.626	0.600	0.579	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns

Table 28: IOB High Performance (HP) Switching Characteristics

I/O Standards	T _{INBUF_DELAY_PAD_I}					T _{OUTBUF_DELAY_O_PAD}					T _{OUTBUF_DELAY_TD_PAD}					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
DIFF_HSTL_I_12_F	0.277	0.335	0.342	0.335	0.321	0.402	0.396	0.414	0.396	0.383	0.402	0.396	0.414	0.396	0.383	ns
DIFF_HSTL_I_12_M	0.277	0.335	0.342	0.335	0.321	0.402	0.395	0.414	0.395	0.383	0.402	0.395	0.414	0.395	0.383	ns
DIFF_HSTL_I_12_S	0.277	0.335	0.342	0.335	0.321	0.402	0.396	0.414	0.396	0.383	0.402	0.396	0.414	0.396	0.383	ns
DIFF_HSTL_I_18_F	0.285	0.314	0.334	0.314	0.328	0.388	0.396	0.413	0.396	0.388	0.388	0.396	0.413	0.396	0.388	ns
DIFF_HSTL_I_18_M	0.285	0.314	0.334	0.314	0.328	0.388	0.393	0.413	0.393	0.389	0.388	0.393	0.413	0.393	0.389	ns
DIFF_HSTL_I_18_S	0.285	0.314	0.334	0.314	0.328	0.388	0.394	0.413	0.391	0.387	0.388	0.394	0.413	0.391	0.387	ns
DIFF_HSTL_I_DCI_12_F	0.277	0.335	0.342	0.335	0.321	0.422	0.420	0.444	0.421	0.414	0.422	0.420	0.444	0.421	0.414	ns
DIFF_HSTL_I_DCI_12_M	0.277	0.335	0.342	0.335	0.321	0.422	0.420	0.444	0.422	0.412	0.422	0.420	0.444	0.422	0.412	ns
DIFF_HSTL_I_DCI_12_S	0.277	0.335	0.342	0.335	0.321	0.422	0.421	0.442	0.421	0.412	0.422	0.421	0.442	0.421	0.412	ns
DIFF_HSTL_I_DCI_18_F	0.284	0.314	0.331	0.314	0.331	0.418	0.425	0.440	0.424	0.417	0.418	0.425	0.440	0.424	0.417	ns
DIFF_HSTL_I_DCI_18_M	0.284	0.314	0.331	0.314	0.331	0.418	0.424	0.443	0.423	0.416	0.418	0.424	0.443	0.423	0.416	ns
DIFF_HSTL_I_DCI_18_S	0.284	0.314	0.331	0.314	0.331	0.418	0.424	0.443	0.424	0.417	0.418	0.424	0.443	0.424	0.417	ns
DIFF_HSTL_I_DCI_F	0.294	0.313	0.330	0.313	0.320	0.420	0.423	0.438	0.421	0.415	0.420	0.423	0.438	0.421	0.415	ns
DIFF_HSTL_I_DCI_M	0.294	0.313	0.330	0.313	0.320	0.420	0.423	0.440	0.423	0.416	0.420	0.423	0.440	0.423	0.416	ns
DIFF_HSTL_I_DCI_S	0.294	0.313	0.330	0.313	0.320	0.420	0.421	0.440	0.417	0.414	0.420	0.421	0.440	0.417	0.414	ns
DIFF_HSTL_I_F	0.295	0.330	0.341	0.330	0.320	0.393	0.391	0.411	0.394	0.385	0.393	0.391	0.411	0.394	0.385	ns
DIFF_HSTL_I_M	0.295	0.330	0.341	0.330	0.320	0.392	0.393	0.413	0.397	0.386	0.392	0.393	0.413	0.397	0.386	ns
DIFF_HSTL_I_S	0.295	0.330	0.341	0.330	0.320	0.393	0.393	0.413	0.394	0.384	0.393	0.393	0.413	0.394	0.384	ns
DIFF_HSUL_12_DCI_F	0.283	0.327	0.344	0.327	0.317	0.428	0.421	0.440	0.421	0.412	0.428	0.421	0.440	0.421	0.412	ns
DIFF_HSUL_12_DCI_M	0.283	0.327	0.344	0.327	0.317	0.428	0.421	0.440	0.421	0.412	0.428	0.421	0.440	0.421	0.412	ns
DIFF_HSUL_12_DCI_S	0.283	0.327	0.344	0.327	0.317	0.428	0.421	0.440	0.421	0.412	0.428	0.421	0.440	0.421	0.412	ns
DIFF_HSUL_12_F	0.277	0.335	0.342	0.335	0.321	0.402	0.396	0.414	0.396	0.383	0.402	0.396	0.414	0.396	0.383	ns
DIFF_HSUL_12_M	0.277	0.335	0.342	0.335	0.321	0.402	0.395	0.414	0.395	0.383	0.402	0.395	0.414	0.395	0.383	ns
DIFF_HSUL_12_S	0.277	0.335	0.342	0.335	0.321	0.402	0.395	0.414	0.395	0.383	0.402	0.395	0.414	0.395	0.383	ns
DIFF_POD10_DCI_F	0.286	0.325	0.340	0.325	0.334	0.438	0.431	0.451	0.431	0.418	0.438	0.431	0.451	0.431	0.418	ns
DIFF_POD10_DCI_M	0.286	0.325	0.340	0.325	0.334	0.592	0.627	0.660	0.627	0.622	0.592	0.627	0.660	0.627	0.622	ns
DIFF_POD10_DCI_S	0.286	0.325	0.340	0.325	0.334	0.823	0.900	0.974	0.900	0.888	0.823	0.900	0.974	0.900	0.888	ns
DIFF_POD10_F	0.277	0.314	0.331	0.314	0.317	0.412	0.406	0.426	0.406	0.392	0.412	0.406	0.426	0.406	0.392	ns
DIFF_POD10_M	0.277	0.314	0.331	0.314	0.317	0.570	0.593	0.627	0.593	0.588	0.570	0.593	0.627	0.593	0.588	ns
DIFF_POD10_S	0.277	0.314	0.331	0.314	0.317	0.800	0.853	0.914	0.853	0.835	0.800	0.853	0.914	0.853	0.835	ns
DIFF_POD12_DCI_F	0.275	0.314	0.333	0.314	0.318	0.428	0.421	0.440	0.421	0.412	0.428	0.421	0.440	0.421	0.412	ns
DIFF_POD12_DCI_M	0.275	0.314	0.333	0.314	0.318	0.586	0.628	0.662	0.628	0.623	0.586	0.628	0.662	0.628	0.623	ns
DIFF_POD12_DCI_S	0.275	0.314	0.333	0.314	0.318	0.813	0.899	0.959	0.899	0.892	0.813	0.899	0.959	0.899	0.892	ns
DIFF_POD12_F	0.275	0.323	0.341	0.323	0.316	0.402	0.396	0.414	0.395	0.383	0.402	0.396	0.414	0.395	0.383	ns
DIFF_POD12_M	0.275	0.323	0.341	0.323	0.316	0.562	0.595	0.629	0.595	0.589	0.562	0.595	0.629	0.595	0.589	ns
DIFF_POD12_S	0.275	0.323	0.341	0.323	0.316	0.789	0.844	0.899	0.844	0.835	0.789	0.844	0.899	0.844	0.835	ns
DIFF_SSTL12_DCI_F	0.283	0.327	0.344	0.327	0.317	0.428	0.421	0.440	0.421	0.412	0.428	0.421	0.440	0.421	0.412	ns
DIFF_SSTL12_DCI_M	0.283	0.327	0.344	0.327	0.317	0.584	0.630	0.664	0.628	0.624	0.584	0.630	0.664	0.628	0.624	ns
DIFF_SSTL12_DCI_S	0.283	0.327	0.344	0.327	0.317	0.813	0.899	0.959	0.899	0.892	0.813	0.899	0.959	0.899	0.892	ns
DIFF_SSTL12_F	0.277	0.335	0.342	0.335	0.321	0.402	0.396	0.414	0.396	0.383	0.402	0.396	0.414	0.396	0.383	ns
DIFF_SSTL12_M	0.277	0.335	0.342	0.335	0.321	0.561	0.597	0.631	0.597	0.591	0.561	0.597	0.631	0.597	0.591	ns

Table 28: IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standards	T _{INBUF_DELAY_PAD_I}					T _{OUTBUF_DELAY_O_PAD}					T _{OUTBUF_DELAY_TD_PAD}					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
DIFF_SSTL12_S	0.277	0.335	0.342	0.335	0.321	0.789	0.844	0.899	0.844	0.835	0.789	0.844	0.899	0.844	0.835	ns
DIFF_SSTL135_DCI_F	0.278	0.312	0.339	0.312	0.319	0.426	0.420	0.439	0.422	0.414	0.426	0.420	0.439	0.422	0.414	ns
DIFF_SSTL135_DCI_M	0.278	0.312	0.339	0.312	0.319	0.586	0.630	0.666	0.630	0.626	0.586	0.630	0.666	0.630	0.626	ns
DIFF_SSTL135_DCI_S	0.278	0.312	0.339	0.312	0.319	0.814	0.902	0.966	0.895	0.896	0.814	0.902	0.966	0.895	0.896	ns
DIFF_SSTL135_F	0.289	0.313	0.336	0.313	0.315	0.397	0.392	0.412	0.394	0.385	0.397	0.392	0.412	0.394	0.385	ns
DIFF_SSTL135_M	0.289	0.313	0.336	0.313	0.315	0.565	0.599	0.633	0.598	0.593	0.565	0.599	0.633	0.598	0.593	ns
DIFF_SSTL135_S	0.289	0.313	0.336	0.313	0.315	0.789	0.850	0.907	0.849	0.841	0.789	0.850	0.907	0.849	0.841	ns
DIFF_SSTL15_DCI_F	0.294	0.313	0.330	0.313	0.320	0.424	0.421	0.439	0.423	0.422	0.424	0.421	0.439	0.423	0.422	ns
DIFF_SSTL15_DCI_M	0.294	0.313	0.330	0.313	0.320	0.591	0.632	0.667	0.632	0.627	0.591	0.632	0.667	0.632	0.627	ns
DIFF_SSTL15_DCI_S	0.294	0.313	0.330	0.313	0.320	0.816	0.906	0.971	0.906	0.898	0.816	0.906	0.971	0.906	0.898	ns
DIFF_SSTL15_F	0.295	0.330	0.341	0.330	0.320	0.393	0.392	0.412	0.392	0.386	0.393	0.392	0.412	0.392	0.386	ns
DIFF_SSTL15_M	0.295	0.330	0.341	0.330	0.320	0.564	0.598	0.633	0.598	0.592	0.564	0.598	0.633	0.598	0.592	ns
DIFF_SSTL15_S	0.295	0.330	0.341	0.330	0.320	0.790	0.853	0.910	0.850	0.844	0.790	0.853	0.910	0.850	0.844	ns
DIFF_SSTL18_I_DCI_F	0.284	0.314	0.331	0.314	0.331	0.418	0.425	0.440	0.424	0.416	0.418	0.425	0.440	0.424	0.416	ns
DIFF_SSTL18_I_DCI_M	0.284	0.314	0.331	0.314	0.331	0.593	0.633	0.670	0.634	0.629	0.593	0.633	0.670	0.634	0.629	ns
DIFF_SSTL18_I_DCI_S	0.284	0.314	0.331	0.314	0.331	0.821	0.910	0.978	0.911	0.903	0.821	0.910	0.978	0.911	0.903	ns
DIFF_SSTL18_I_F	0.285	0.314	0.334	0.314	0.328	0.388	0.395	0.415	0.392	0.387	0.388	0.395	0.415	0.392	0.387	ns
DIFF_SSTL18_I_M	0.285	0.314	0.334	0.314	0.328	0.567	0.603	0.638	0.603	0.596	0.567	0.603	0.638	0.603	0.596	ns
DIFF_SSTL18_I_S	0.285	0.314	0.334	0.314	0.328	0.794	0.861	0.920	0.860	0.851	0.794	0.861	0.920	0.860	0.851	ns
HSLVDCI_15_F	0.343	0.364	0.384	0.364	0.360	0.424	0.422	0.440	0.421	0.418	0.424	0.422	0.440	0.421	0.418	ns
HSLVDCI_15_M	0.343	0.364	0.384	0.364	0.360	0.424	0.420	0.441	0.424	0.413	0.424	0.420	0.441	0.424	0.413	ns
HSLVDCI_15_S	0.343	0.364	0.384	0.364	0.360	0.424	0.421	0.440	0.421	0.417	0.424	0.421	0.440	0.421	0.417	ns
HSLVDCI_18_F	0.343	0.365	0.386	0.365	0.361	0.420	0.425	0.440	0.424	0.416	0.420	0.425	0.440	0.424	0.416	ns
HSLVDCI_18_M	0.343	0.365	0.386	0.365	0.361	0.423	0.424	0.440	0.423	0.418	0.423	0.424	0.440	0.423	0.418	ns
HSLVDCI_18_S	0.343	0.365	0.386	0.365	0.361	0.420	0.423	0.443	0.425	0.414	0.420	0.423	0.443	0.425	0.414	ns
HSTL_I_12_F	0.342	0.363	0.384	0.363	0.360	0.402	0.396	0.414	0.396	0.383	0.402	0.396	0.414	0.396	0.383	ns
HSTL_I_12_M	0.342	0.363	0.384	0.363	0.360	0.402	0.395	0.414	0.395	0.383	0.402	0.395	0.414	0.395	0.383	ns
HSTL_I_12_S	0.342	0.363	0.384	0.363	0.360	0.402	0.396	0.414	0.396	0.383	0.402	0.396	0.414	0.396	0.383	ns
HSTL_I_18_F	0.343	0.365	0.386	0.365	0.361	0.388	0.396	0.413	0.396	0.388	0.388	0.396	0.413	0.396	0.388	ns
HSTL_I_18_M	0.343	0.365	0.386	0.365	0.361	0.388	0.393	0.413	0.393	0.389	0.388	0.393	0.413	0.393	0.389	ns
HSTL_I_18_S	0.343	0.365	0.386	0.365	0.361	0.388	0.394	0.413	0.391	0.387	0.388	0.394	0.413	0.391	0.387	ns
HSTL_I_DCI_12_F	0.342	0.363	0.384	0.363	0.360	0.422	0.420	0.444	0.421	0.414	0.422	0.420	0.444	0.421	0.414	ns
HSTL_I_DCI_12_M	0.342	0.363	0.384	0.363	0.360	0.422	0.420	0.444	0.422	0.412	0.422	0.420	0.444	0.422	0.412	ns
HSTL_I_DCI_12_S	0.342	0.363	0.384	0.363	0.360	0.422	0.421	0.442	0.421	0.412	0.422	0.421	0.442	0.421	0.412	ns
HSTL_I_DCI_18_F	0.343	0.365	0.386	0.365	0.361	0.418	0.425	0.440	0.424	0.417	0.418	0.425	0.440	0.424	0.417	ns
HSTL_I_DCI_18_M	0.343	0.365	0.386	0.365	0.361	0.418	0.424	0.443	0.423	0.416	0.418	0.424	0.443	0.423	0.416	ns
HSTL_I_DCI_18_S	0.343	0.365	0.386	0.365	0.361	0.418	0.424	0.443	0.424	0.417	0.418	0.424	0.443	0.424	0.417	ns
HSTL_I_DCI_F	0.343	0.364	0.384	0.364	0.360	0.420	0.423	0.438	0.421	0.415	0.420	0.423	0.438	0.421	0.415	ns
HSTL_I_DCI_M	0.343	0.364	0.384	0.364	0.360	0.420	0.423	0.440	0.423	0.416	0.420	0.423	0.440	0.423	0.416	ns
HSTL_I_DCI_S	0.343	0.364	0.384	0.364	0.360	0.420	0.421	0.440	0.417	0.414	0.420	0.421	0.440	0.417	0.414	ns
HSTL_I_F	0.342	0.363	0.384	0.363	0.360	0.393	0.391	0.411	0.394	0.385	0.393	0.391	0.411	0.394	0.385	ns

Table 28: IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standards	T _{INBUF_DELAY_PAD_I}					T _{OUTBUF_DELAY_O_PAD}					T _{OUTBUF_DELAY_TD_PAD}					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
HSTL_I_M	0.342	0.363	0.384	0.363	0.360	0.392	0.393	0.413	0.397	0.386	0.392	0.393	0.413	0.397	0.386	ns
HSTL_I_S	0.342	0.363	0.384	0.363	0.360	0.393	0.393	0.413	0.394	0.384	0.393	0.393	0.413	0.394	0.384	ns
HSUL_12_DCI_F	0.343	0.363	0.384	0.363	0.360	0.428	0.421	0.440	0.421	0.412	0.428	0.421	0.440	0.421	0.412	ns
HSUL_12_DCI_M	0.343	0.363	0.384	0.363	0.360	0.428	0.421	0.440	0.421	0.412	0.428	0.421	0.440	0.421	0.412	ns
HSUL_12_DCI_S	0.343	0.363	0.384	0.363	0.360	0.428	0.421	0.440	0.421	0.412	0.428	0.421	0.440	0.421	0.412	ns
HSUL_12_F	0.342	0.363	0.384	0.363	0.360	0.402	0.396	0.414	0.396	0.383	0.402	0.396	0.414	0.396	0.383	ns
HSUL_12_M	0.342	0.363	0.384	0.363	0.360	0.402	0.395	0.414	0.395	0.383	0.402	0.395	0.414	0.395	0.383	ns
HSUL_12_S	0.342	0.363	0.384	0.363	0.360	0.402	0.395	0.414	0.395	0.383	0.402	0.395	0.414	0.395	0.383	ns
LVC MOS12_F_2	0.476	0.552	0.600	0.552	0.557	0.865	0.841	0.867	0.839	0.820	0.865	0.841	0.867	0.839	0.820	ns
LVC MOS12_F_4	0.476	0.552	0.600	0.552	0.557	0.640	0.642	0.665	0.635	0.624	0.640	0.642	0.665	0.635	0.624	ns
LVC MOS12_F_6	0.476	0.552	0.600	0.552	0.557	0.533	0.515	0.540	0.515	0.502	0.533	0.515	0.540	0.515	0.502	ns
LVC MOS12_F_8	0.476	0.552	0.600	0.552	0.557	0.476	0.472	0.498	0.477	0.461	0.476	0.472	0.498	0.477	0.461	ns
LVC MOS12_M_2	0.476	0.552	0.600	0.552	0.557	0.904	0.899	0.923	0.893	0.881	0.904	0.899	0.923	0.893	0.881	ns
LVC MOS12_M_4	0.476	0.552	0.600	0.552	0.557	0.740	0.741	0.773	0.741	0.733	0.740	0.741	0.773	0.741	0.733	ns
LVC MOS12_M_6	0.476	0.552	0.600	0.552	0.557	0.634	0.655	0.690	0.657	0.648	0.634	0.655	0.690	0.657	0.648	ns
LVC MOS12_M_8	0.476	0.552	0.600	0.552	0.557	0.633	0.672	0.712	0.672	0.665	0.633	0.672	0.712	0.672	0.665	ns
LVC MOS12_S_2	0.476	0.552	0.600	0.552	0.557	0.974	0.976	1.022	0.976	0.963	0.974	0.976	1.022	0.976	0.963	ns
LVC MOS12_S_4	0.476	0.552	0.600	0.552	0.557	0.861	0.902	0.956	0.902	0.888	0.861	0.902	0.956	0.902	0.888	ns
LVC MOS12_S_6	0.476	0.552	0.600	0.552	0.557	0.821	0.890	0.943	0.890	0.876	0.821	0.890	0.943	0.890	0.876	ns
LVC MOS12_S_8	0.476	0.552	0.600	0.552	0.557	0.871	0.947	1.020	0.947	0.939	0.871	0.947	1.020	0.947	0.939	ns
LVC MOS15_F_12	0.395	0.443	0.478	0.443	0.439	0.422	0.417	0.436	0.417	0.408	0.422	0.417	0.436	0.417	0.408	ns
LVC MOS15_F_2	0.395	0.443	0.478	0.443	0.439	0.847	0.837	0.861	0.832	0.819	0.847	0.837	0.861	0.832	0.819	ns
LVC MOS15_F_4	0.395	0.443	0.478	0.443	0.439	0.637	0.633	0.658	0.633	0.621	0.637	0.633	0.658	0.633	0.621	ns
LVC MOS15_F_6	0.395	0.443	0.478	0.443	0.439	0.517	0.511	0.532	0.511	0.501	0.517	0.511	0.532	0.511	0.501	ns
LVC MOS15_F_8	0.395	0.443	0.478	0.443	0.439	0.472	0.469	0.488	0.468	0.457	0.472	0.469	0.488	0.468	0.457	ns
LVC MOS15_M_12	0.395	0.443	0.478	0.443	0.439	0.669	0.73	0.775	0.73	0.723	0.669	0.73	0.775	0.73	0.723	ns
LVC MOS15_M_2	0.395	0.443	0.478	0.443	0.439	0.898	0.895	0.93	0.895	0.883	0.898	0.895	0.93	0.895	0.883	ns
LVC MOS15_M_4	0.395	0.443	0.478	0.443	0.439	0.726	0.743	0.774	0.743	0.731	0.726	0.743	0.774	0.743	0.731	ns
LVC MOS15_M_6	0.395	0.443	0.478	0.443	0.439	0.633	0.658	0.691	0.659	0.642	0.633	0.658	0.691	0.659	0.642	ns
LVC MOS15_M_8	0.395	0.443	0.478	0.443	0.439	0.635	0.673	0.714	0.673	0.669	0.635	0.673	0.714	0.673	0.669	ns
LVC MOS15_S_12	0.395	0.443	0.478	0.443	0.439	1.002	1.119	1.216	1.122	1.112	1.002	1.119	1.216	1.122	1.112	ns
LVC MOS15_S_2	0.395	0.443	0.478	0.443	0.439	0.967	0.979	1.022	0.977	0.965	0.967	0.979	1.022	0.977	0.965	ns
LVC MOS15_S_4	0.395	0.443	0.478	0.443	0.439	0.861	0.907	0.959	0.907	0.894	0.861	0.907	0.959	0.907	0.894	ns
LVC MOS15_S_6	0.395	0.443	0.478	0.443	0.439	0.825	0.898	0.950	0.898	0.885	0.825	0.898	0.950	0.898	0.885	ns
LVC MOS15_S_8	0.395	0.443	0.478	0.443	0.439	0.871	0.955	1.026	0.953	0.943	0.871	0.955	1.026	0.953	0.943	ns
LVC MOS18_F_12	0.352	0.388	0.414	0.388	0.377	0.412	0.418	0.440	0.418	0.410	0.412	0.418	0.440	0.418	0.410	ns
LVC MOS18_F_2	0.352	0.388	0.414	0.388	0.377	0.850	0.841	0.865	0.841	0.828	0.850	0.841	0.865	0.841	0.828	ns
LVC MOS18_F_4	0.352	0.388	0.414	0.388	0.377	0.643	0.637	0.660	0.637	0.624	0.643	0.637	0.660	0.637	0.624	ns
LVC MOS18_F_6	0.352	0.388	0.414	0.388	0.377	0.507	0.506	0.532	0.506	0.501	0.507	0.506	0.532	0.506	0.501	ns
LVC MOS18_F_8	0.352	0.388	0.414	0.388	0.377	0.468	0.468	0.491	0.468	0.459	0.468	0.468	0.491	0.468	0.459	ns
LVC MOS18_M_12	0.352	0.388	0.414	0.388	0.377	0.681	0.734	0.779	0.734	0.727	0.681	0.734	0.779	0.734	0.727	ns

Table 28: IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standards	T _{INBUF_DELAY_PAD_I}					T _{OUTBUF_DELAY_O_PAD}					T _{OUTBUF_DELAY_TD_PAD}					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
LVC MOS18_M_2	0.352	0.388	0.414	0.388	0.377	0.902	0.899	0.927	0.899	0.884	0.902	0.899	0.927	0.899	0.884	ns
LVC MOS18_M_4	0.352	0.388	0.414	0.388	0.377	0.731	0.745	0.778	0.745	0.731	0.731	0.745	0.778	0.745	0.731	ns
LVC MOS18_M_6	0.352	0.388	0.414	0.388	0.377	0.638	0.659	0.696	0.664	0.653	0.638	0.659	0.696	0.664	0.653	ns
LVC MOS18_M_8	0.352	0.388	0.414	0.388	0.377	0.632	0.678	0.717	0.678	0.667	0.632	0.678	0.717	0.678	0.667	ns
LVC MOS18_S_12	0.352	0.388	0.414	0.388	0.377	1.015	1.130	1.224	1.130	1.119	1.015	1.130	1.224	1.130	1.119	ns
LVC MOS18_S_2	0.352	0.388	0.414	0.388	0.377	0.967	0.983	1.024	0.984	0.967	0.967	0.983	1.024	0.984	0.967	ns
LVC MOS18_S_4	0.352	0.388	0.414	0.388	0.377	0.864	0.910	0.964	0.910	0.897	0.864	0.910	0.964	0.910	0.897	ns
LVC MOS18_S_6	0.352	0.388	0.414	0.388	0.377	0.836	0.900	0.957	0.900	0.888	0.836	0.900	0.957	0.900	0.888	ns
LVC MOS18_S_8	0.352	0.388	0.414	0.388	0.377	0.881	0.959	1.033	0.959	0.948	0.881	0.959	1.033	0.959	0.948	ns
LVDCI_15_F	0.392	0.436	0.476	0.436	0.437	0.424	0.422	0.441	0.418	0.415	0.424	0.422	0.441	0.418	0.415	ns
LVDCI_15_M	0.392	0.436	0.476	0.436	0.437	0.591	0.632	0.666	0.632	0.628	0.591	0.632	0.666	0.632	0.628	ns
LVDCI_15_S	0.392	0.436	0.476	0.436	0.437	0.815	0.906	0.972	0.905	0.898	0.815	0.906	0.972	0.905	0.898	ns
LVDCI_18_F	0.346	0.376	0.407	0.376	0.374	0.418	0.425	0.443	0.425	0.418	0.418	0.425	0.443	0.425	0.418	ns
LVDCI_18_M	0.346	0.376	0.407	0.376	0.374	0.594	0.633	0.670	0.633	0.628	0.594	0.633	0.670	0.633	0.628	ns
LVDCI_18_S	0.346	0.376	0.407	0.376	0.374	0.821	0.908	0.978	0.908	0.902	0.821	0.908	0.978	0.908	0.902	ns
LVDS	0.315	0.352	0.406	0.352	0.348	0.392	0.404	0.425	0.404	0.396	0.392	0.404	0.425	0.404	0.396	ns
MIPI_DPHY_DCI_HS	0.305	0.317	0.342	0.317	0.319	0.429	0.434	0.452	0.434	0.427	N/A	N/A	N/A	N/A	N/A	ns
MIPI_DPHY_DCI_LP	8.477	8.423	8.777	8.415	8.698	1.627	1.604	1.642	1.604	1.583	N/A	N/A	N/A	N/A	N/A	ns
POD10_DCI_F	0.342	0.363	0.384	0.363	0.360	0.438	0.431	0.451	0.431	0.418	0.438	0.431	0.451	0.431	0.418	ns
POD10_DCI_M	0.342	0.363	0.384	0.363	0.360	0.592	0.627	0.660	0.627	0.622	0.592	0.627	0.660	0.627	0.622	ns
POD10_DCI_S	0.342	0.363	0.384	0.363	0.360	0.823	0.900	0.974	0.900	0.888	0.823	0.900	0.974	0.900	0.888	ns
POD10_F	0.343	0.363	0.384	0.363	0.360	0.412	0.406	0.426	0.406	0.392	0.412	0.406	0.426	0.406	0.392	ns
POD10_M	0.343	0.363	0.384	0.363	0.360	0.570	0.593	0.627	0.593	0.588	0.570	0.593	0.627	0.593	0.588	ns
POD10_S	0.343	0.363	0.384	0.363	0.360	0.800	0.853	0.914	0.853	0.835	0.800	0.853	0.914	0.853	0.835	ns
POD12_DCI_F	0.343	0.364	0.386	0.364	0.360	0.428	0.421	0.440	0.421	0.412	0.428	0.421	0.440	0.421	0.412	ns
POD12_DCI_M	0.343	0.364	0.386	0.364	0.360	0.586	0.628	0.662	0.628	0.623	0.586	0.628	0.662	0.628	0.623	ns
POD12_DCI_S	0.343	0.364	0.386	0.364	0.360	0.813	0.899	0.959	0.899	0.892	0.813	0.899	0.959	0.899	0.892	ns
POD12_F	0.343	0.364	0.386	0.364	0.360	0.402	0.396	0.414	0.395	0.383	0.402	0.396	0.414	0.395	0.383	ns
POD12_M	0.343	0.364	0.386	0.364	0.360	0.562	0.595	0.629	0.595	0.589	0.562	0.595	0.629	0.595	0.589	ns
POD12_S	0.343	0.364	0.386	0.364	0.360	0.789	0.844	0.899	0.844	0.835	0.789	0.844	0.899	0.844	0.835	ns
SLVS_400_18	0.315	0.352	0.406	0.352	0.348	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_DCI_F	0.331	0.366	0.384	0.366	0.350	0.428	0.421	0.440	0.421	0.412	0.428	0.421	0.440	0.421	0.412	ns
SSTL12_DCI_M	0.331	0.366	0.384	0.366	0.350	0.584	0.630	0.664	0.628	0.624	0.584	0.630	0.664	0.628	0.624	ns
SSTL12_DCI_S	0.331	0.366	0.384	0.366	0.350	0.813	0.899	0.959	0.899	0.892	0.813	0.899	0.959	0.899	0.892	ns
SSTL12_F	0.333	0.377	0.375	0.377	0.343	0.402	0.396	0.414	0.396	0.383	0.402	0.396	0.414	0.396	0.383	ns
SSTL12_M	0.333	0.377	0.375	0.377	0.343	0.561	0.597	0.631	0.597	0.591	0.561	0.597	0.631	0.597	0.591	ns
SSTL12_S	0.333	0.377	0.375	0.377	0.343	0.789	0.844	0.899	0.844	0.835	0.789	0.844	0.899	0.844	0.835	ns
SSTL135_DCI_F	0.341	0.351	0.384	0.351	0.367	0.426	0.420	0.439	0.422	0.414	0.426	0.420	0.439	0.422	0.414	ns
SSTL135_DCI_M	0.341	0.351	0.384	0.351	0.367	0.586	0.630	0.666	0.630	0.626	0.586	0.630	0.666	0.630	0.626	ns
SSTL135_DCI_S	0.341	0.351	0.384	0.351	0.367	0.814	0.902	0.966	0.895	0.896	0.814	0.902	0.966	0.895	0.896	ns
SSTL135_F	0.331	0.352	0.373	0.352	0.356	0.397	0.392	0.412	0.394	0.385	0.397	0.392	0.412	0.394	0.385	ns

Table 28: IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standards	T _{INBUF_DELAY_PAD_I}					T _{OUTBUF_DELAY_O_PAD}					T _{OUTBUF_DELAY_TD_PAD}					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
SSTL135_M	0.331	0.352	0.373	0.352	0.356	0.565	0.599	0.633	0.598	0.593	0.565	0.599	0.633	0.598	0.593	ns
SSTL135_S	0.331	0.352	0.373	0.352	0.356	0.789	0.850	0.907	0.849	0.841	0.789	0.850	0.907	0.849	0.841	ns
SSTL15_DCI_F	0.332	0.349	0.362	0.349	0.346	0.424	0.421	0.439	0.423	0.422	0.424	0.421	0.439	0.423	0.422	ns
SSTL15_DCI_M	0.332	0.349	0.362	0.349	0.346	0.591	0.632	0.667	0.632	0.627	0.591	0.632	0.667	0.632	0.627	ns
SSTL15_DCI_S	0.332	0.349	0.362	0.349	0.346	0.816	0.906	0.971	0.906	0.898	0.816	0.906	0.971	0.906	0.898	ns
SSTL15_F	0.32	0.356	0.385	0.356	0.353	0.393	0.392	0.412	0.392	0.386	0.393	0.392	0.412	0.392	0.386	ns
SSTL15_M	0.32	0.356	0.385	0.356	0.353	0.564	0.598	0.633	0.598	0.592	0.564	0.598	0.633	0.598	0.592	ns
SSTL15_S	0.32	0.356	0.385	0.356	0.353	0.790	0.853	0.910	0.85	0.844	0.790	0.853	0.910	0.85	0.844	ns
SSTL18_I_DCI_F	0.333	0.353	0.360	0.353	0.347	0.418	0.425	0.440	0.424	0.416	0.418	0.425	0.440	0.424	0.416	ns
SSTL18_I_DCI_M	0.333	0.353	0.360	0.353	0.347	0.593	0.633	0.670	0.634	0.629	0.593	0.633	0.670	0.634	0.629	ns
SSTL18_I_DCI_S	0.333	0.353	0.360	0.353	0.347	0.821	0.910	0.978	0.911	0.903	0.821	0.910	0.978	0.911	0.903	ns
SSTL18_I_F	0.323	0.355	0.378	0.355	0.364	0.388	0.395	0.415	0.392	0.387	0.388	0.395	0.415	0.392	0.387	ns
SSTL18_I_M	0.323	0.355	0.378	0.355	0.364	0.567	0.603	0.638	0.603	0.596	0.567	0.603	0.638	0.603	0.596	ns
SSTL18_I_S	0.323	0.355	0.378	0.355	0.364	0.794	0.861	0.920	0.860	0.851	0.794	0.861	0.920	0.860	0.851	ns
SUB_LVDS	0.315	0.352	0.406	0.352	0.348	0.387	0.398	0.418	0.398	0.390	0.387	0.398	0.418	0.398	0.390	ns

Table 29 specifies the values of T_{OUTBUF_DELAY_TE_PAD} and T_{INBUF_DELAY_IBUFDIS_O}. T_{OUTBUF_DELAY_TE_PAD} is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). T_{INBUF_DELAY_IBUFDIS_O} is the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than T_{OUTBUF_DELAY_TE_PAD} when the DCITERMDISABLE pin is used. In HD I/O banks, the internal IN_TERM termination turn-off time is always faster than T_{OUTBUF_DELAY_TE_PAD} when the INTERMDISABLE pin is used.

Table 29: IOB 3-state Output Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V		0.85V		0.72V	
		-3	-2	-1	-2	-1	
T _{OUTBUF_DELAY_TE_PAD}	T input to pad high-impedance for HD I/O banks						ns
	T input to pad high-impedance for HP I/O banks						ns
T _{INBUF_DELAY_IBUFDIS_O}	IBUF turn-on time from IBUFDISABLE to O output for HD I/O banks						ns
	IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks						ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 30 shows the test setup parameters used for measuring input delay.

Table 30: Input Delay Measurement Methodology

Description	I/O Standard Attribute	$V_L^{(1)(2)}$	$V_H^{(1)(2)}$	$V_{MEAS}^{(1)(4)(6)}$	$V_{REF}^{(1)(3)(5)}$
LVC MOS, 1.2V	LVC MOS12	0.1	1.1	0.6	–
LVC MOS, LVDCI, HSLVDCI, 1.5V	LVC MOS15, LVDCI_15, HSLVDCI_15	0.1	1.4	0.75	–
LVC MOS, LVDCI, HSLVDCI, 1.8V	LVC MOS18, LVDCI_18, HSLVDCI_18	0.1	1.7	0.9	–
LVC MOS, 2.5V	LVC MOS25	0.1	2.4	1.25	–
LVC MOS, 3.3V	LVC MOS33	0.1	3.2	1.65	–
LV TTL, 3.3V	LV TTL	0.1	3.2	1.65	–
HSTL (high-speed transceiver logic), class I, 1.2V	HSTL_I_12	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.6
HSTL, class I, 1.5V	HSTL_I	$V_{REF} - 0.65$	$V_{REF} + 0.65$	V_{REF}	0.75
HSTL, class I, 1.8V	HSTL_I_18	$V_{REF} - 0.8$	$V_{REF} + 0.8$	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.6
SSTL12 (stub series terminated logic), 1.2V	SSTL12	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.6
SSTL135 and SSTL135 class II, 1.35V	SSTL135, SSTL135_II	$V_{REF} - 0.575$	$V_{REF} + 0.575$	V_{REF}	0.675
SSTL15 and SSTL15 class II, 1.5V	SSTL15, SSTL15_II	$V_{REF} - 0.65$	$V_{REF} + 0.65$	V_{REF}	0.75
SSTL18, class I and II, 1.8V	SSTL18_I, SSTL18_II	$V_{REF} - 0.8$	$V_{REF} + 0.8$	V_{REF}	0.9
POD10, 1.0V	POD10	$V_{REF} - 0.6$	$V_{REF} + 0.6$	V_{REF}	0.7
POD12, 1.2V	POD12	$V_{REF} - 0.74$	$V_{REF} + 0.74$	V_{REF}	0.84
DIFF_HSTL, class I, 1.2V	DIFF_HSTL_I_12	$0.6 - 0.125$	$0.6 + 0.125$	$0^{(6)}$	–
DIFF_HSTL, class I, 1.5V	DIFF_HSTL_I	$0.75 - 0.125$	$0.75 + 0.125$	$0^{(6)}$	–
DIFF_HSTL, class I, 1.8V	DIFF_HSTL_I_18	$0.9 - 0.125$	$0.9 + 0.125$	$0^{(6)}$	–
DIFF_HSUL, 1.2V	DIFF_HSUL_12	$0.6 - 0.125$	$0.6 + 0.125$	$0^{(6)}$	–
DIFF_SSTL, 1.2V	DIFF_SSTL12	$0.6 - 0.125$	$0.6 + 0.125$	$0^{(6)}$	–
DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V	DIFF_SSTL135, DIFF_SSTL135_II	$0.675 - 0.125$	$0.675 + 0.125$	$0^{(6)}$	–
DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V	DIFF_SSTL15, DIFF_SSTL15_II	$0.75 - 0.125$	$0.75 + 0.125$	$0^{(6)}$	–
DIFF_SSTL18_I, DIFF_SSTL18_II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	$0.9 - 0.125$	$0.9 + 0.125$	$0^{(6)}$	–
DIFF_POD10, 1.0V	DIFF_POD10	$0.7 - 0.125$	$0.7 + 0.125$	$0^{(6)}$	–
DIFF_POD12, 1.2V	DIFF_POD12	$0.84 - 0.125$	$0.84 + 0.125$	$0^{(6)}$	–
LVDS (low-voltage differential signaling), 1.8V	LVDS	$0.9 - 0.125$	$0.9 + 0.125$	$0^{(6)}$	–

Table 30: Input Delay Measurement Methodology (Cont'd)

Description	I/O Standard Attribute	$V_L^{(1)(2)}$	$V_H^{(1)(2)}$	$V_{MEAS}^{(1)(4)(6)}$	$V_{REF}^{(1)(3)(5)}$
LVDS_25, 2.5V	LVDS_25	1.25 – 0.125	1.25 + 0.125	0 ⁽⁶⁾	–
SUB_LVDS, 1.8V	SUB_LVDS	0.9 – 0.125	0.9 + 0.125	0 ⁽⁶⁾	–
SLVS, 1.8V	SLVS_400_18	0.9 – 0.125	0.9 + 0.125	0 ⁽⁶⁾	–
SLVS, 2.5V	SLVS_400_25	1.25 – 0.125	1.25 + 0.125	0 ⁽⁶⁾	–
LVPECL, 2.5V	LVPECL	1.25 – 0.125	1.25 + 0.125	0 ⁽⁶⁾	–
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	0.2 – 0.125	0.2 + 0.125	0 ⁽⁶⁾	–
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	0.715 – 0.2	0.715 + 0.2	0 ⁽⁶⁾	–

Notes:

1. The input delay measurement methodology parameters for LVDCI/HSLVDCI are the same for LVCMOS standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H .
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF}/V_{MEAS} parameters found in IBIS models and/or noted in [Figure 1](#).
6. The value given is the differential input voltage.

Output Delay Measurements

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in [Figure 1](#) and [Figure 2](#).

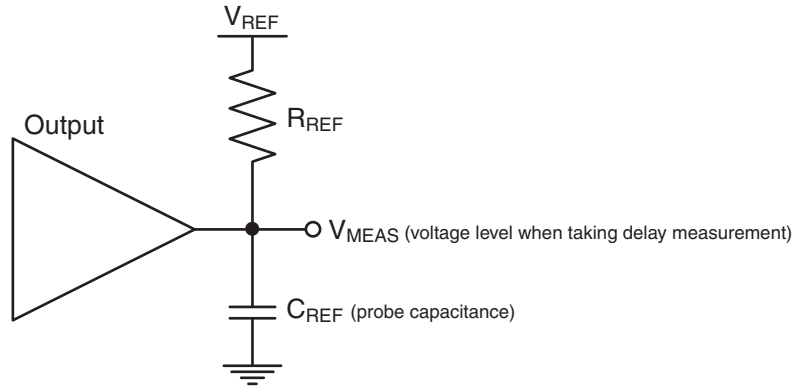


Figure 1: Single-Ended Test Setup

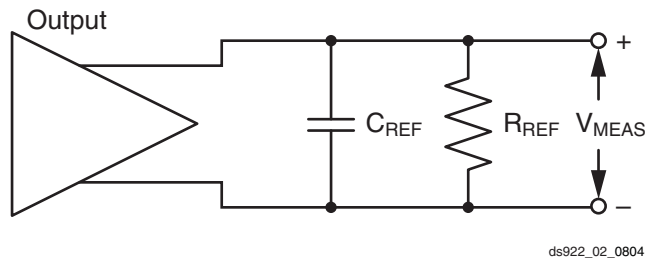


Figure 2: Differential Test Setup

Parameters V_{REF} , R_{REF} , C_{REF} , and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from [Table 31](#).
2. Record the time to V_{MEAS} .
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS} .
5. Compare the results of [step 2](#) and [step 4](#). The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 31: Output Delay Measurement Methodology

Description	I/O Standard Attribute	R _{REF} (Ω)	C _{REF} ⁽¹⁾ (pF)	V _{MEAS} (V)	V _{REF} (V)
LVC MOS, 1.2V	LVC MOS12	1M	0	0.6	0
LVC MOS, 1.5V	LVC MOS15	1M	0	0.75	0
LVC MOS, 1.8V	LVC MOS18	1M	0	0.9	0
LVC MOS, 2.5V	LVC MOS25	1M	0	1.25	0
LVC MOS, 3.3V	LVC MOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
LVDCI, HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	50	0	V _{REF}	0.75
LVDCI, HSLVDCI, 1.8V	LVDCI_15, HSLVDCI_18	50	0	V _{REF}	0.9
HSTL (high-speed transceiver logic), class I, 1.2V	HSTL_I_12	50	0	V _{REF}	0.6
HSTL, class I, 1.5V	HSTL_I	50	0	V _{REF}	0.75
HSTL, class I, 1.8V	HSTL_I_18	50	0	V _{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	50	0	V _{REF}	0.6
SSTL12 (stub series terminated logic), 1.2V	SSTL12	50	0	V _{REF}	0.6
SSTL135 and SSTL135 class II, 1.35V	SSTL135, SSTL135_II	50	0	V _{REF}	0.675
SSTL15 and SSTL15 class II, 1.5V	SSTL15, SSTL15_II	50	0	V _{REF}	0.75
SSTL18, class I and class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V _{REF}	0.9
POD10, 1.0V	POD10	50	0	V _{REF}	1.0
POD12, 1.2V	POD12	50	0	V _{REF}	1.2
DIFF_HSTL, class I, 1.2V	DIFF_HSTL_I_12	50	0	V _{REF}	0.6
DIFF_HSTL, class I, 1.5V	DIFF_HSTL_I	50	0	V _{REF}	0.75
DIFF_HSTL, class I, 1.8V	DIFF_HSTL_I_18	50	0	V _{REF}	0.9
DIFF_HSUL, 1.2V	DIFF_HSUL_12	50	0	V _{REF}	0.6
DIFF_SSTL12, 1.2V	DIFF_SSTL12	50	0	V _{REF}	0.6
DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V	DIFF_SSTL135, DIFF_SSTL135_II	50	0	V _{REF}	0.675
DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V	DIFF_SSTL15, DIFF_SSTL15_II	50	0	V _{REF}	0.75
DIFF_SSTL18, class I and II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V _{REF}	0.9
DIFF_POD10, 1.0V	DIFF_POD10	50	0	V _{REF}	1.0
DIFF_POD12, 1.2V	DIFF_POD12	50	0	V _{REF}	1.2
LVDS (low-voltage differential signaling), 1.8V	LVDS	100	0	0 ⁽²⁾	0
SUB_LVDS, 1.8V	SUB_LVDS	100	0	0 ⁽²⁾	0
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	100	0	0 ⁽²⁾	0
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	1M	0	0.6	0

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Block RAM and FIFO Switching Characteristics

Table 32: Block RAM and FIFO Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Maximum Frequency							
F _{MAX_WF_NC}	Block RAM (WRITE_FIRST and NO_CHANGE modes).	825	737	645	585	516	MHz
F _{MAX_RF}	Block RAM (READ_FIRST mode).	718	637	575	510	460	MHz
F _{MAX_FIFO}	FIFO in all modes without ECC.	825	737	645	585	516	MHz
F _{MAX_ECC}	Block RAM and FIFO in ECC configuration without PIPELINE.	718	637	575	510	460	MHz
	Block RAM and FIFO in ECC configuration with PIPELINE and Block RAM in WRITE_FIRST or NO_CHANGE mode.	825	737	645	585	516	MHz
T _{PW} ⁽¹⁾	Minimum pulse width.	495	542	543	577	578	ps
Block RAM and FIFO Clock-to-Out Delays							
T _{RCKO_DO}	Clock CLK to DOUT output (without output register).	0.92	1.03	1.11	1.46	1.54	ns, Max
T _{RCKO_DO_REG}	Clock CLK to DOUT output (with output register).	0.27	0.29	0.31	0.42	0.44	ns, Max

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

UltraRAM Switching Characteristics

The *UltraScale Architecture and Product Overview* ([DS890](#)) lists the Kintex UltraScale+ FPGAs that include this memory.

Table 33: UltraRAM Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Maximum Frequency							
F _{MAX}	UltraRAM maximum frequency with OREG_B.	650	600	600	500	500	MHz
F _{MAX_ECC}	UltraRAM maximum frequency without OREG_B and EN_ECC_RD_B = True.	450	400	400	325	325	MHz
F _{MAX_NORPIPELINE}	UltraRAM maximum frequency with OREG_B = False and EN_ECC_RD_B = False.	550	500	500	425	425	MHz
T _{PW} ⁽¹⁾	Minimum pulse width.	650	700	700	800	800	ps
T _{RSTPW}	Asynchronous reset minimum pulse width.	550	600	600	650	650	ps

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

Input/Output Delay Switching Characteristics

Table 34: Input/Output Delay Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
F _{REFCLK}	REFCLK frequency (component mode).	200 to 800					MHz
	REFCLK frequency (native mode).	200 to 2400	200 to 2400	200 to 2133			MHz
T _{MINPER_RST}	Minimum reset pulse width.	52.00					ns
T _{IDELAY_RESOLUTION} / T _{ODELAY_RESOLUTION}	IDELAY/ODELAY chain resolution.	2.5 to 15					ps

DSP48 Slice Switching Characteristics

Table 35: DSP48 Slice Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Maximum Frequency							
F _{MAX}	With all registers used.	891	775	645	644	600	MHz
F _{MAX_PATDET}	With pattern detector.	794	687	571	562	524	MHz
F _{MAX_MULT_NOMREG}	Two register multiply without MREG.	635	544	456	440	413	MHz
F _{MAX_MULT_NOMREG_PATDET}	Two register multiply without MREG with pattern detect.	577	492	410	395	371	MHz
F _{MAX_PREADD_NOADREG}	Without ADREG.	655	565	468	453	423	MHz
F _{MAX_NOPIPELINEREG}	Without pipeline registers (MREG, ADREG).	483	410	338	323	304	MHz
F _{MAX_NOPIPELINEREG_PATDET}	Without pipeline registers (MREG, ADREG) with pattern detect.	448	379	314	299	280	MHz

Clock Buffers and Networks

Table 36: Clock Buffers Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Global Clock Switching Characteristics (Including BUFGCTRL)							
F _{MAX}	Maximum frequency of a global clock tree (BUFG).	891	775	667	725	667	MHz
Global Clock Buffer with Input Divide Capability (BUFGCE_DIV)							
F _{MAX}	Maximum frequency of a global clock buffer with input divide capability (BUFGCE_DIV).	891	775	667	725	667	MHz
Global Clock Buffer with Clock Enable (BUFGCE)							
F _{MAX}	Maximum frequency of a global clock buffer with clock enable (BUFGCE).	891	775	667	725	667	MHz
Leaf Clock Buffer with Clock Enable (BUFCE_LEAF)							
F _{MAX}	Maximum frequency of a leaf clock buffer with clock enable (BUFCE_LEAF).	891	775	667	725	667	MHz
GTH or GTY Clock Buffer with Clock Enable and Clock Input Divide Capability (BUFG_GT)							
F _{MAX}	Maximum frequency of a serial transceiver clock buffer with clock enable and clock input divide capability.	512	512	512	512	512	MHz

MMCM Switching Characteristics

Table 37: MMCM Specification

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
MMCM_F _{INMAX}	Maximum input clock frequency.	1066	933	800	933	800	MHz
MMCM_F _{INMIN}	Minimum input clock frequency.	10	10	10	10	10	MHz
MMCM_F _{INJITTER}	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max					
MMCM_F _{INDUTY}	Input duty cycle range: 10–49 MHz.	25–75					%
	Input duty cycle range: 50–199 MHz.	30–70					%
	Input duty cycle range: 200–399 MHz.	35–65					%
	Input duty cycle range: 400–499 MHz.	40–60					%
	Input duty cycle range: >500 MHz.	45–55					%
MMCM_F _{MIN_PSCLK}	Minimum dynamic phase shift clock frequency.	0.01	0.01	0.01	0.01	0.01	MHz
MMCM_F _{MAX_PSCLK}	Maximum dynamic phase shift clock frequency.	550	500	450	500	450	MHz
MMCM_F _{VCOMIN}	Minimum MMCM VCO frequency.	800	800	800	800	800	MHz
MMCM_F _{VCOMAX}	Maximum MMCM VCO frequency.	1600	1600	1600	1600	1600	MHz
MMCM_F _{BANDWIDTH}	Low MMCM bandwidth at typical. ⁽¹⁾	1.00	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical. ⁽¹⁾	4.00	4.00	4.00	4.00	4.00	MHz
MMCM_T _{STATPHAOFFSET}	Static phase offset of the MMCM outputs. ⁽²⁾	0.12	0.12	0.12	0.12	0.12	ns
MMCM_T _{OUTJITTER}	MMCM output jitter.	Note 3					
MMCM_T _{OUTDUTY}	MMCM output clock duty cycle precision. ⁽⁴⁾	0.165	0.20	0.20	0.20	0.20	ns
MMCM_T _{LOCKMAX}	MMCM maximum lock time for MMCM_F _{PFDMIN} .	100	100	100	100	100	μs
MMCM_F _{OUTMAX}	MMCM maximum output frequency.	891	775	667	725	667	MHz
MMCM_F _{OUTMIN}	MMCM minimum output frequency. ⁽⁴⁾⁽⁵⁾	6.25	6.25	6.25	6.25	6.25	MHz
MMCM_T _{EXTFDVAR}	External clock feedback variation.	< 20% of clock input period or 1 ns Max					
MMCM_RST _{MINPULSE}	Minimum reset pulse width.	5.00	5.00	5.00	5.00	5.00	ns
MMCM_F _{PFDMAX}	Maximum frequency at the phase frequency detector.	550	500	450	500	450	MHz
MMCM_F _{PFDMIN}	Minimum frequency at the phase frequency detector.	10	10	10	10	10	MHz
MMCM_T _{FBDELAY}	Maximum delay in the feedback path.	5 ns Max or one clock cycle					

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

PLL Switching Characteristics

 Table 38: PLL Specification⁽¹⁾

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V		0.85V		0.72V	
		-3	-2	-1	-2	-1	
PLL_F _{INMAX}	Maximum input clock frequency.	1066	933	800	933	800	MHz
PLL_F _{INMIN}	Minimum input clock frequency.	70	70	70	70	70	MHz
PLL_F _{INJITTER}	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max					
PLL_F _{INDUTY}	Input duty cycle range: 70–399 MHz.	35–65					%
	Input duty cycle range: 400–499 MHz.	40–60					%
	Input duty cycle range: >500 MHz.	45–55					%
PLL_F _{VCOMIN}	Minimum PLL VCO frequency.	750	750	750	750	750	MHz
PLL_F _{VCOMAX}	Maximum PLL VCO frequency.	1500	1500	1500	1500	1500	MHz
PLL_T _{STATPHAOFFSET}	Static phase offset of the PLL outputs. ⁽²⁾	0.12	0.12	0.12	0.12	0.12	ns
PLL_T _{OUTJITTER}	PLL output jitter.	Note 3					
PLL_T _{OUTDUTY}	PLL CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B duty-cycle precision. ⁽⁴⁾	0.165	0.20	0.20	0.20	0.20	ns
PLL_T _{LOCKMAX}	PLL maximum lock time.	100					µs
PLL_F _{OUTMAX}	PLL maximum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B.	891	775	667	725	667	MHz
	PLL maximum output frequency at CLKOUTPHY.	2667	2667	2400	2400	2133	MHz
PLL_F _{OUTMIN}	PLL minimum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B. ⁽⁵⁾	5.86	5.86	5.86	5.86	5.86	MHz
	PLL minimum output frequency at CLKOUTPHY.	2 x VCO mode: 1500, 1 x VCO mode: 750 0.5 x VCO mode: 375					MHz
PLL_RST _{MINPULSE}	Minimum reset pulse width.	5.00	5.00	5.00	5.00	5.00	ns
PLL_F _{PFDMAX}	Maximum frequency at the phase frequency detector.	667.5	667.5	667.5	667.5	667.5	MHz
PLL_F _{PFDMIN}	Minimum frequency at the phase frequency detector.	70	70	70	70	70	MHz
PLL_F _{BANDWIDTH}	PLL bandwidth at typical.	14	14	14	14	14	MHz

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the loop filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

Device Pin-to-Pin Output Parameter Guidelines

The pin-to-pin numbers in [Table 39](#) through [Table 41](#) are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 39: Global Clock Input to Output Delay Without MMCM (Near Clock Region)

Symbol	Description	Device	Speed Grade and V _{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, without MMCM.								
T _{ICKOF}	Global clock input and output flip-flop <i>without</i> MMCM (near clock region).	XCKU3P	4.59	4.96	5.37	5.72	6.08	ns
		XCKU5P	4.59	4.96	5.37	5.72	6.08	ns
		XCKU9P	5.42	5.76	6.16	7.10	7.16	ns
		XCKU11P	5.93	6.43	6.87	7.47	7.96	ns
		XCKU13P	5.49	6.05	6.57	7.28	7.82	ns
		XCKU15P	6.27	6.77	7.22	7.94	8.42	ns

Notes:

- This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.

Table 40: Global Clock Input to Output Delay Without MMCM (Far Clock Region)

Symbol	Description	Device	Speed Grade and V _{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, without MMCM.								
T _{ICKOF_FAR}	Global clock input and output flip-flop <i>without</i> MMCM (far clock region).	XCKU3P	4.76	5.18	5.61	5.97	6.39	ns
		XCKU5P	4.76	5.18	5.61	5.97	6.39	ns
		XCKU9P	5.62	5.98	6.38	7.39	7.46	ns
		XCKU11P	6.28	6.79	7.24	7.97	8.45	ns
		XCKU13P	5.69	6.30	6.83	7.60	8.17	ns
		XCKU15P	6.79	7.31	7.79	8.68	9.16	ns

Notes:

- This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.

Table 41: Global Clock Input to Output Delay With MMCM

Symbol	Description	Device	Speed Grade and V _{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with MMCM.								
T _{ICKOFMMCMCC}	Global clock input and output flip-flop <i>with</i> MMCM.	XCKU3P	2.33	2.44	2.62	2.84	2.89	ns
		XCKU5P	2.33	2.44	2.62	2.84	2.89	ns
		XCKU9P	2.75	2.82	3.01	3.49	3.43	ns
		XCKU11P	2.64	2.80	3.04	3.23	3.39	ns
		XCKU13P	2.77	2.82	3.08	3.43	3.53	ns
		XCKU15P	2.78	2.99	3.25	3.39	3.64	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.
2. MMCM output jitter is already included in the timing calculation.

Device Pin-to-Pin Input Parameter Guidelines

The pin-to-pin numbers in [Table 42](#) and [Table 43](#) are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 42: Global Clock Input Setup and Hold With 3.3V HD I/O without MMCM

Symbol	Description	Device	Speed Grade and V _{CCINT} Operating Voltages					Units	
			0.90V	0.85V		0.72V			
			-3	-2	-1	-2	-1		
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard. ⁽¹⁾⁽²⁾⁽³⁾									
T _{PSFD_KU3P}	Global clock input and input flip-flop (or latch) without MMCM.	Setup	XCKU3P	-0.69	-0.69	-0.69	-0.85	-0.85	ns
T _{PHFD_KU3P}		Hold	XCKU3P	1.88	2.09	2.20	2.60	2.82	ns
T _{PSFD_KU5P}		Setup	XCKU5P	-0.69	-0.69	-0.69	-0.85	-0.85	ns
T _{PHFD_KU5P}		Hold	XCKU5P	1.88	2.09	2.20	2.60	2.82	ns
T _{PSFD_KU9P}		Setup	XCKU9P	-1.06	-1.06	-1.06	-1.06	-1.06	ns
T _{PHFD_KU9P}		Hold	XCKU9P	2.40	2.59	2.71	3.47	3.54	ns
T _{PSFD_KU11P}		Setup	XCKU11P	-0.72	-0.72	-0.72	-0.89	-0.89	ns
T _{PHFD_KU11P}		Hold	XCKU11P	1.91	2.14	2.25	2.64	2.88	ns
T _{PSFD_KU13P}		Setup	XCKU13P	-1.07	-1.07	-1.07	-1.24	-1.24	ns
T _{PHFD_KU13P}		Hold	XCKU13P	2.39	2.74	2.94	3.53	3.91	ns
T _{PSFD_KU15P}		Setup	XCKU15P	-0.79	-0.79	-0.79	-0.98	-0.98	ns
T _{PHFD_KU15P}		Hold	XCKU15P	2.08	2.31	2.43	2.87	3.11	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 43: Global Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grade and V _{CCINT} Operating Voltages					Units	
			0.90V	0.85V		0.72V			
			-3	-2	-1	-2	-1		
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard. (1)(2)(3)									
T _{PSMMCMCC_KU3P}	Global clock input and input flip-flop (or latch) with MMCM.	Setup	XCKU3P	2.24	2.49	2.66	2.69	2.69	ns
T _{PHMMCMCC_KU3P}		Hold	XCKU3P	0.23	0.23	0.23	0.32	0.39	ns
T _{PSMMCMCC_KU5P}		Setup	XCKU5P	2.24	2.49	2.66	2.69	2.69	ns
T _{PHMMCMCC_KU5P}		Hold	XCKU5P	0.23	0.23	0.23	0.32	0.39	ns
T _{PSMMCMCC_KU9P}		Setup	XCKU9P	1.88	2.04	2.19	2.19	2.19	ns
T _{PHMMCMCC_KU9P}		Hold	XCKU9P	0.42	0.42	0.42	0.71	0.71	ns
T _{PSMMCMCC_KU11P}		Setup	XCKU11P	1.91	2.14	2.33	2.33	2.33	ns
T _{PHMMCMCC_KU11P}		Hold	XCKU11P	0.25	0.25	0.25	0.37	0.50	ns
T _{PSMMCMCC_KU13P}		Setup	XCKU13P	1.88	2.08	2.26	2.29	2.29	ns
T _{PHMMCMCC_KU13P}		Hold	XCKU13P	0.36	0.36	0.36	0.50	0.64	ns
T _{PSMMCMCC_KU15P}		Setup	XCKU15P	1.88	2.11	2.28	2.28	2.28	ns
T _{PHMMCMCC_KU15P}		Hold	XCKU15P	0.33	0.31	0.31	0.49	0.58	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 44: Sampling Window

Description	Speed Grade and V _{CCINT} Operating Voltages					Units
	0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	
T _{SAMP_BUFG} ⁽¹⁾						ps
T _{SAMP_NATIVE_DPA}						ps
T _{SAMP_NATIVE_BISC}						ps

Notes:

1. This parameter indicates the total sampling error of the Kintex UltraScale+ FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include: CLK0 MMCM jitter, MMCM accuracy (phase offset), and MMCM phase shift resolution. These measurements do not include package or clock tree skew.

Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for clock transmitter and receiver data-valid windows.

Table 45: Package Skew

Symbol	Description	Device	Package	Value	Units
PKGSKEW	Package Skew	XCKU3P	SFVB784		ps
			FFVA676		ps
			FFVB676		ps
			FFVD900		ps
		XCKU5P	SFVB784		ps
			FFVA676		ps
			FFVB676		ps
			FFVD900		ps
		XCKU9P	FFVE900	212	ps
		XCKU11P	FFVD900		ps
			FFVA1156		ps
			FFVE1517		ps
		XCKU13P	FFVE900		ps
		XCKU15P	FFVA1156		ps
			FFVE1517		ps
			FFVA1760		ps
FFVE1760			ps		

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

GTH Transceiver Specifications

The *UltraScale Architecture and Product Overview* ([DS890](#)) lists the Kintex UltraScale+ FPGAs that include the GTH transceivers.

GTH Transceiver DC Input and Output Levels

[Table 46](#) summarizes the DC specifications of the GTH transceivers in the Kintex UltraScale+ FPGAs. Consult the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) for further details.

Table 46: GTH Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV _{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	> 10.3125 Gb/s		–		mV
		6.6 Gb/s to 10.3125 Gb/s		–		mV
		≤ 6.6 Gb/s		–		mV
V _{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled V _{MGTAVTT} = 1.2V		–	V _{MGTAVTT}	mV
V _{CMIN}	Common mode input voltage	DC coupled V _{MGTAVTT} = 1.2V	–	2/3 V _{MGTAVTT}	–	mV
D _{VPPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to 1010		–	–	mV
V _{CMOUTDC}	Common mode output voltage: DC coupled (equation based)	When remote RX is terminated to GND	$V_{MGTAVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V _{RX_TERM} ⁽²⁾	$V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX_TERM}}{2}\right)$			mV
V _{CMOUTAC}	Common mode output voltage: AC coupled (equation based)		$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R _{IN}	Differential input resistance		–	100	–	Ω
R _{OUT}	Differential output resistance		–	100	–	Ω
T _{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (All packages)		–	–	10	ps
C _{EXT}	Recommended external AC coupling capacitor ⁽³⁾		–		–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the attributes discussed in the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)), and can result in values lower than reported in this table.
2. V_{RX_TERM} is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.

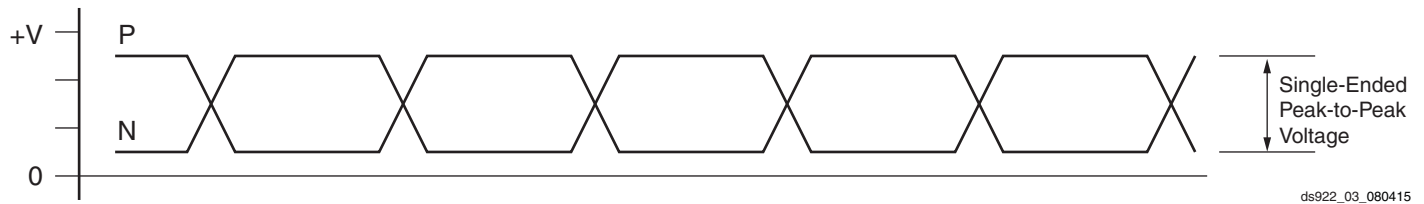


Figure 3: Single-Ended Peak-to-Peak Voltage

ds922_03_080415

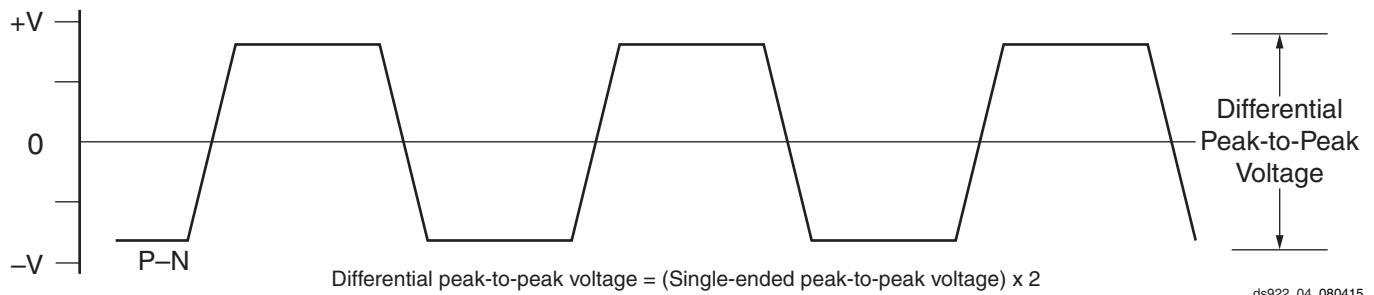


Figure 4: Differential Peak-to-Peak Voltage

ds922_04_080415

Table 47 and Table 48 summarize the DC specifications of the GTH transceivers input and output clocks in Kintex UltraScale+ FPGAs. Consult the *UltraScale Architecture GTH Transceiver User Guide (UG576)* for further details.

Table 47: GTH Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V _{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R _{IN}	Differential input resistance	–	100	–	Ω
C _{EXT}	Required external AC coupling capacitor	–	10	–	nF

Table 48: GTH Transceiver Clock Output Level Specification

Symbol	Description	Conditions	Min	Typ	Max	Units
V _{OL}	Output high voltage for P and N	R _T = 100Ω across P and N signals	–		–	mV
V _{OH}	Output low voltage for P and N	R _T = 100Ω across P and N signals	–		–	mV
V _{DDOUT}	Differential output voltage (P–N), P = High (N–P), N = High	R _T = 100Ω across P and N signals	–		–	mV
V _{CMOUT}	Common mode voltage	R _T = 100Ω across P and N signals	–		–	mV

GTH Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) for further information.

Table 49: GTH Transceiver Performance

Symbol	Description	Output Divider	Speed Grade and V _{CCINT} Operating Voltages										Units
			0.90V		0.85V				0.72V				
			-3		-2		-1		-2		-1		
F _{GTHMAX}	GTH maximum line rate.		16.375		16.375				12.5				Gb/s
F _{GTHMIN}	GTH minimum line rate.		0.5		0.5				0.5				Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTHCRANGE}	CPLL line rate range ⁽¹⁾ .	1	4	12.5	4	12.5	4	8.5	4	8.5	4	8.5	Gb/s
		2	2	6.25	2	6.25	2	4.25	2	4.25	2	4.25	Gb/s
		4	1	3.125	1	3.125	1	2.125	1	2.125	1	2.125	Gb/s
		8	0.5	1.5625	0.5	1.5625	0.5	1.0625	0.5	1.0625	0.5	1.0625	Gb/s
		16	N/A										Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTHQRANGE1}	QPLL0 line rate range ⁽²⁾ .	1	9.8	16.375	9.8	16.375	9.8	12.5	9.8	12.5	9.8	10.3125	Gb/s
		2	4.9	8.1875	4.9	8.1875	4.9	8.15	4.9	8.1875	4.9	8.15	Gb/s
		4	2.45	4.09375	2.45	4.09375	2.45	4.075	2.45	4.09375	2.45	4.075	Gb/s
		8	1.225	2.04688	1.225	2.04688	1.225	2.0375	1.225	2.04688	1.225	2.0375	Gb/s
		16	0.6125	1.02344	0.6125	1.02344	0.6125	1.01875	0.6125	1.02344	0.6125	1.01875	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTHQRANGE2}	QPLL1 line rate range ⁽³⁾ .	1	8.0	13	8.0	13	8.0	12.5	8.0	12.5	8.0	10.3125	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{CPLLRANGE}	CPLL frequency range.		2	6.25	2	6.25	2	4.25	2	4.25	2	4.25	GHz
F _{QPLLORANGE}	QPLL0 frequency range.		9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	GHz
F _{QPLL1RANGE}	QPLL1 frequency range.		8	13	8	13	8	13	8	13	8	13	GHz

Notes:

1. The values listed are the rounded results of the calculated equation $(2 \times \text{CPLL_Frequency}) / \text{Output_Divider}$.
2. The values listed are the rounded results of the calculated equation $(\text{QPLL0_Frequency}) / \text{Output_Divider}$.
3. The values listed are the rounded results of the calculated equation $(\text{QPLL1_Frequency}) / \text{Output_Divider}$.

Table 50: GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	All Speed Grades	Units
F _{GTHDRPCLK}	GTHDRPCLK maximum frequency.		MHz

Table 51: GTH Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range.		60	–	820	MHz
T_{RCLK}	Reference clock rise time.	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time.	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle.	Transceiver PLL only	40	50	60	%

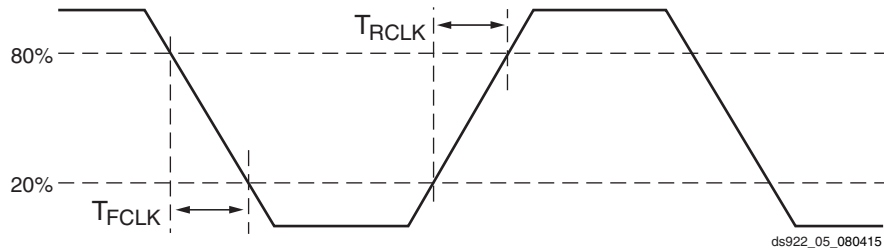


Figure 5: Reference Clock Timing Parameters

Table 52: GTH Transceiver Reference Clock Oscillator Selection Phase Noise Mask

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
$QPLL_{REFCLKMASK}^{(1)(2)}$	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–105	dBc/Hz
		100 kHz	–	–	–124	
		1 MHz	–	–	–130	
$CPLL_{REFCLKMASK}^{(1)(2)}$	CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–105	dBc/Hz
		100 kHz	–	–	–124	
		1 MHz	–	–	–130	
		50 MHz	–	–	–140	

Notes:

- For reference clock frequencies other than 312.5 MHz, adjust the phase-noise mask values by $20 \times \log(N/312.5)$ where N is the new reference clock frequency in MHz.
- This reference clock phase-noise mask is superseded by any reference clock phase-noise mask that is specified in a supported protocol, e.g., PCIe.

Table 53: GTH Transceiver PLL/Lock Time Adaptation

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock.		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–			UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–			UI

Table 54: GTH Transceiver User Clock Switching Characteristics⁽¹⁾

Symbol	Description	Data Width Conditions (Bit)		Speed Grade, Temperature Ranges, and V _{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
		Internal Logic	Interconnect Logic	-3 ⁽²⁾	-2 ⁽²⁾⁽³⁾	-1 ⁽⁴⁾	-2 ⁽³⁾	-1 ⁽³⁾⁽⁵⁾	
F _{TXOUTPMA}	TXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	390.625	390.625	322.266	MHz
F _{RXOUTPMA}	RXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	390.625	390.625	322.266	MHz
F _{TXOUTPROGDIV}	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
F _{RXOUTPROGDIV}	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
F _{TXIN}	TXUSRCLK maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	312.500	257.813	MHz
F _{RXIN}	RXUSRCLK maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	312.500	257.813	MHz
F _{TXIN2}	TXUSRCLK2 maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	312.500	257.813	MHz
		40	80	204.688	204.688	156.250	156.250	128.906	MHz
F _{RXIN2}	RXUSRCLK2 maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	312.500	257.813	MHz
		40	80	204.688	204.688	156.250	156.250	128.906	MHz

Notes:

1. Clocking must be implemented as described in *UltraScale Architecture GTH Transceiver User Guide* (UG576).
2. For speed grades -3E and -2I, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s.
3. For speed grade -2LE, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s when V_{CCINT} = 0.85V or 6.25 Gb/s when V_{CCINT} = 0.72V.
4. For speed grades -1E and -1I, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s.
5. For speed grade -1LI, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s when V_{CCINT} = 0.85V or 5.15625 Gb/s when V_{CCINT} = 0.72V.

Table 55: GTH Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTHTX}	Serial data rate range		0.500	–	F_{GTHMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	40	–	ps
T_{FTX}	TX fall time	80%–20%	–	40	–	ps
T_{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–		ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–		mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–		ns
$T_{J16.375}$	Total jitter ⁽²⁾⁽⁴⁾	16.375 Gb/s	–	–		UI
$D_{J16.375}$	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–		UI
$T_{J15.1}$	Total jitter ⁽²⁾⁽⁴⁾	15.1 Gb/s	–	–		UI
$D_{J15.1}$	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–		UI
$T_{J14.1}$	Total jitter ⁽²⁾⁽⁴⁾	14.1 Gb/s	–	–		UI
$D_{J14.1}$	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–		UI
$T_{J13.1}$	Total jitter ⁽²⁾⁽⁴⁾	13.1 Gb/s	–	–		UI
$D_{J13.1}$	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–		UI
$T_{J12.5}$	Total jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	–	–		UI
$D_{J12.5}$	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–		UI
$T_{J11.3}$	Total jitter ⁽²⁾⁽⁴⁾	11.3 Gb/s	–	–		UI
$D_{J11.3}$	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–		UI
$T_{J10.3125_QPLL}$	Total jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	–	–		UI
$D_{J10.3125_QPLL}$	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–		UI
$T_{J10.3125_CPLL}$	Total jitter ⁽³⁾⁽⁴⁾	10.3125 Gb/s	–	–		UI
$D_{J10.3125_CPLL}$	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–		UI
$T_{J9.953}$	Total jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	–	–		UI
$D_{J9.953}$	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–		UI
$T_{J8.0_QPLL}$	Total jitter ⁽²⁾⁽⁴⁾	8.0 Gb/s	–	–		UI
$D_{J8.0_QPLL}$	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–		UI
$T_{J8.0_CPLL}$	Total jitter ⁽³⁾⁽⁴⁾	8.0 Gb/s	–	–		UI
$D_{J8.0_CPLL}$	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–		UI
$T_{J6.6_CPLL}$	Total jitter ⁽³⁾⁽⁴⁾	6.6 Gb/s	–	–		UI
$D_{J6.6_CPLL}$	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–		UI
$T_{J5.0}$	Total jitter ⁽³⁾⁽⁴⁾	5.0 Gb/s	–	–		UI
$D_{J5.0}$	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–		UI
$T_{J4.25}$	Total jitter ⁽³⁾⁽⁴⁾	4.25 Gb/s	–	–		UI
$D_{J4.25}$	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–		UI
$T_{J3.75}$	Total jitter ⁽³⁾⁽⁴⁾	3.75 Gb/s	–	–		UI
$D_{J3.75}$	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–		UI
$T_{J3.20}$	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁵⁾	–	–		UI
$D_{J3.20}$	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–		UI
$T_{J3.20L}$	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁶⁾	–	–		UI
$D_{J3.20L}$	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–		UI

Table 55: GTH Transceiver Transmitter Switching Characteristics (Cont'd)

Symbol	Description	Condition	Min	Typ	Max	Units
T _{J2.5}	Total jitter ⁽³⁾⁽⁴⁾	2.5 Gb/s ⁽⁷⁾	–	–		UI
D _{J2.5}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–		UI
T _{J1.25}	Total jitter ⁽³⁾⁽⁴⁾	1.25 Gb/s ⁽⁸⁾	–	–		UI
D _{J1.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–		UI
T _{J500}	Total jitter ⁽³⁾⁽⁴⁾	500 Mb/s	–	–		UI
D _{J500}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–		UI

Notes:

- Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTH Quad) at the maximum line rate.
- Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 10⁻¹².
- CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
- CPLL frequency at 1.6 GHz and TXOUT_DIV = 1.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.

Table 56: GTH Transceiver Receiver Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTHRX}	Serial data rate		0.500	–	F _{GTHMAX}	Gb/s
T _{RXELECIDLE}	Time for RXELECIDLE to respond to loss or restoration of data		–	10	–	ns
R _{XOVBVDP}	OOB detect threshold peak-to-peak			–		mV
R _{XSS}	Receiver spread-spectrum tracking ⁽¹⁾	Modulated at 33 kHz		–	0	ppm
R _{XRL}	Run length (CID)		–	–		UI
R _{XPPMTOL}	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s		–		ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s		–		ppm
		Bit rates > 8.0 Gb/s		–		ppm

SJ Jitter Tolerance⁽²⁾

J _{T_SJ16.375}	Sinusoidal jitter (QPLL) ⁽³⁾	16.375 Gb/s		–	–	UI
J _{T_SJ15.1}	Sinusoidal jitter (QPLL) ⁽³⁾	15.1 Gb/s		–	–	UI
J _{T_SJ14.1}	Sinusoidal jitter (QPLL) ⁽³⁾	14.1 Gb/s		–	–	UI
J _{T_SJ13.1}	Sinusoidal jitter (QPLL) ⁽³⁾	13.1 Gb/s		–	–	UI
J _{T_SJ12.5}	Sinusoidal jitter (QPLL) ⁽³⁾	12.5 Gb/s		–	–	UI
J _{T_SJ11.3}	Sinusoidal jitter (QPLL) ⁽³⁾	11.3 Gb/s		–	–	UI
J _{T_SJ10.32_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	10.32 Gb/s		–	–	UI
J _{T_SJ10.32_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	10.32 Gb/s		–	–	UI
J _{T_SJ9.953}	Sinusoidal jitter (QPLL) ⁽³⁾	9.953 Gb/s		–	–	UI
J _{T_SJ8.0_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	8.0 Gb/s		–	–	UI
J _{T_SJ8.0_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	8.0 Gb/s		–	–	UI
J _{T_SJ6.6_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	6.6 Gb/s		–	–	UI

Table 56: GTH Transceiver Receiver Switching Characteristics (Cont'd)

Symbol	Description	Condition	Min	Typ	Max	Units
J _{T_SJ} 5.0	Sinusoidal jitter (CPLL) ⁽³⁾	5.0 Gb/s		–	–	UI
J _{T_SJ} 4.25	Sinusoidal jitter (CPLL) ⁽³⁾	4.25 Gb/s		–	–	UI
J _{T_SJ} 3.75	Sinusoidal jitter (CPLL) ⁽³⁾	3.75 Gb/s		–	–	UI
J _{T_SJ} 3.2	Sinusoidal jitter (CPLL) ⁽³⁾	3.2 Gb/s ⁽⁴⁾		–	–	UI
J _{T_SJ} 3.2L	Sinusoidal jitter (CPLL) ⁽³⁾	3.2 Gb/s ⁽⁵⁾				
J _{T_SJ} 2.5	Sinusoidal jitter (CPLL) ⁽³⁾	2.5 Gb/s ⁽⁶⁾		–	–	UI
J _{T_SJ} 1.25	Sinusoidal jitter (CPLL) ⁽³⁾	1.25 Gb/s ⁽⁷⁾		–	–	UI
J _{T_SJ} 500	Sinusoidal jitter (CPLL) ⁽³⁾	500 Mb/s		–	–	UI
SJ Jitter Tolerance with Stressed Eye⁽²⁾						
J _{T_TJSE} 3.2	Total jitter with stressed eye ⁽⁸⁾	3.2 Gb/s		–	–	UI
J _{T_TJSE} 6.6		6.6 Gb/s		–	–	UI
J _{T_SJSE} 3.2	Sinusoidal jitter with stressed eye ⁽⁸⁾	3.2 Gb/s		–	–	UI
J _{T_SJSE} 6.6		6.6 Gb/s		–	–	UI

Notes:

- Using RXOUT_DIV = 1, 2, and 4.
- All jitter values are based on a bit error ratio of 10⁻¹².
- The frequency of the injected sinusoidal jitter is 80 MHz.
- CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
- CPLL frequency at 1.6 GHz and RXOUT_DIV = 1.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
- Composite jitter with RX equalizer enabled. DFE disabled.

GTH Transceiver Electrical Compliance

The *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) contains recommended use modes that ensure compliance for the protocols listed in [Table 57](#). The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 57: GTH Transceiver Protocol List

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11G-SR	4.25–12.5	Compliant
PCIe Gen1, 2, 3	PCI Express base 3.0	2.5, 5.0, and 8.0	Compliant
SDI	SMPTE 424M-2006	0.27–2.97	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort (source only)	DP 1.2B CTS	1.62–5.4	Compliant
Fibre channel	FC-PI-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625–12.5	Compliant

GTH Transceiver Protocol Jitter Characteristics

For [Table 58](#) through [Table 63](#), the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) contains recommended settings for optimal usage of protocol specific characteristics.

Table 58: Gigabit Ethernet Protocol Characteristics (GTH Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	1250	–		UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250		–	UI

Table 59: XAUI Protocol Characteristics (GTH Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	3125	–		UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125		–	UI

Table 60: PCI Express Protocol Characteristics (GTH Transceivers)⁽¹⁾

Standard	Description	Condition	Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation						
PCI Express Gen 1	Total transmitter jitter		2500	–		UI
PCI Express Gen 2	Total transmitter jitter		5000	–		UI
PCI Express Gen 3 ⁽²⁾	Total transmitter jitter uncorrelated		8000	–		ps
	Deterministic transmitter jitter uncorrelated			–		ps
PCI Express Receiver High Frequency Jitter Tolerance						
PCI Express Gen 1	Total receiver jitter tolerance		2500		–	UI
PCI Express Gen 2 ⁽²⁾	Receiver inherent timing error		5000		–	UI
	Receiver inherent deterministic timing error				–	UI
PCI Express Gen 3 ⁽²⁾	Receiver sinusoidal jitter tolerance	0.03 MHz–1.0 MHz	8000		–	UI
		1.0 MHz–10 MHz		Note 3	–	UI
		10 MHz–100 MHz			–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. Using common REFCLK.
3. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20 dB/decade.

Table 61: CEI-6G and CEI-11G Protocol Characteristics (GTH Transceivers)

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter ⁽¹⁾	4976–6375	CEI-6G-SR	–		UI
		CEI-6G-LR	–		UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance ⁽¹⁾	4976–6375	CEI-6G-SR		–	UI
		CEI-6G-LR		–	UI
CEI-11G Transmitter Jitter Generation					
Total transmitter jitter ⁽²⁾	9950–11100	CEI-11G-SR	–		UI
		CEI-11G-LR/MR	–		UI
CEI-11G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance ⁽²⁾	9950–11100	CEI-11G-SR		–	UI
		CEI-11G-MR		–	UI
		CEI-11G-LR		–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.
2. Tested at line rate of 9950 Mb/s using 155.46875 MHz reference clock and 11100 Mb/s using 173.4375 MHz reference clock.

Table 62: SFP+ Protocol Characteristics (GTH Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
SFP+ Transmitter Jitter Generation				
Total transmitter jitter	9830.40 ⁽¹⁾	–		UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			
SFP+ Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	9830.40 ⁽¹⁾		–	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			

Notes:

1. Line rated used for CPRI over SFP+ applications.

Table 63: CPRI Protocol Characteristics (GTH Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–		UI
	1228.8	–		UI
	2457.6	–		UI
	3072.0	–		UI
	4915.2	–		UI
	6144.0	–		UI
	9830.4	–	Note 1	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4		–	UI
	1228.8		–	UI
	2457.6		–	UI
	3072.0		–	UI
	4915.2		–	UI
	6144.0		–	UI
	9830.4	Note 1	–	UI

Notes:

1. Tested per SFP+ specification, see [Table 62](#).

GTY Transceiver Specifications

The *UltraScale Architecture and Product Overview* ([DS890](#)) lists the Kintex UltraScale+ FPGAs that include the GTY transceivers.

GTY Transceiver DC Input and Output Levels

Table 64 summarizes the DC specifications of the GTY transceivers in Kintex UltraScale+ FPGAs. Consult www.xilinx.com/products/technology/high-speed-serial for further details.

Table 64: GTY Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV _{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	> 10.3125 Gb/s		–		mV
		6.6 Gb/s to 10.3125 Gb/s		–		mV
		≤ 6.6 Gb/s		–		mV
V _{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled V _{MGTAVTT} = 1.2V		–	V _{MGTAVTT}	mV
V _{CMIN}	Common mode input voltage	DC coupled V _{MGTAVTT} = 1.2V	–	2/3 V _{MGTAVTT}	–	mV
D _{VPPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to 1010		–	–	mV
V _{CMOUTDC}	Common mode output voltage: DC coupled (equation based)	When remote RX is terminated to GND	$V_{MGTAVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V _{RX_TERM} ⁽²⁾	$V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX_TERM}}{2}\right)$			mV
V _{CMOUTAC}	Common mode output voltage: AC coupled	Equation based	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R _{IN}	Differential input resistance		–	100	–	Ω
R _{OUT}	Differential output resistance		–	100	–	Ω
T _{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	–	10	ps
C _{EXT}	Recommended external AC coupling capacitor ⁽³⁾		–	100	–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the GTY transceiver attributes discussed in the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) and can result in values lower than reported in this table.
2. V_{RX_TERM} is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.

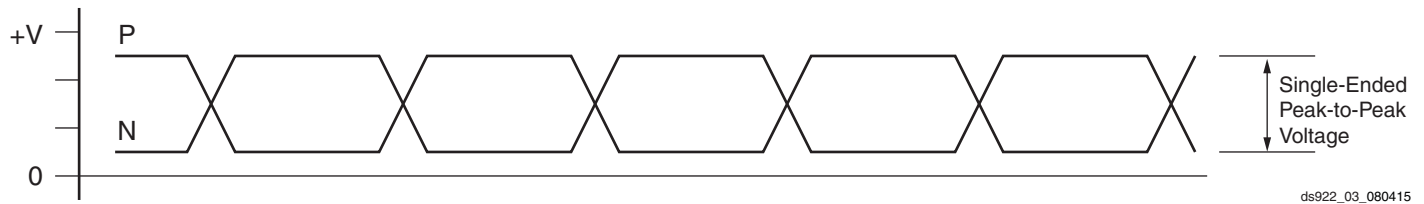


Figure 6: Single-Ended Peak-to-Peak Voltage

ds922_03_080415

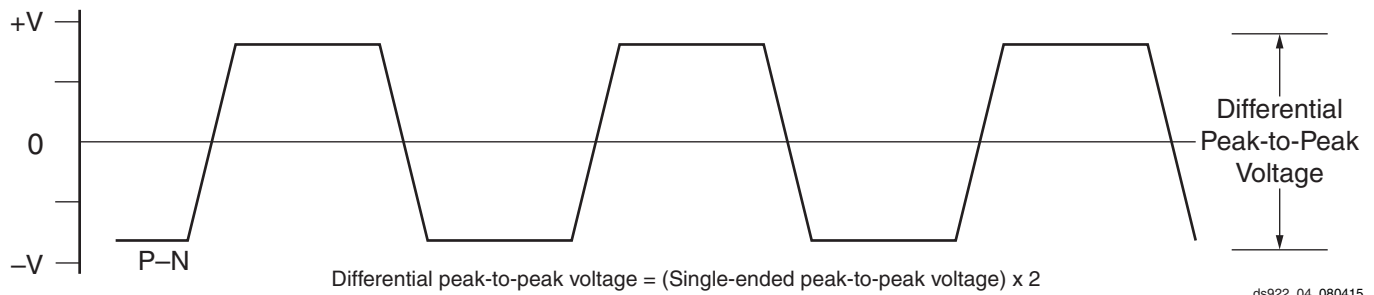


Figure 7: Differential Peak-to-Peak Voltage

ds922_04_080415

Table 65 summarizes the DC specifications of the clock input of the GTY transceivers in Kintex UltraScale+ FPGAs. Consult www.xilinx.com/products/technology/high-speed-serial for further details.

Table 65: GTY Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V _{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R _{IN}	Differential input resistance	–	100	–	Ω
C _{EXT}	Required external AC coupling capacitor	–	10	–	nF

Table 66: GTY Transceiver Clock Output Level Specification

Symbol	Description	Conditions	Min	Typ	Max	Units
V _{OL}	Output high voltage for P and N	R _T = 100Ω across P and N signals	–		–	mV
V _{OH}	Output low voltage for P and N	R _T = 100Ω across P and N signals	–		–	mV
V _{DDOUT}	Differential output voltage (P–N), P = High (N–P), N = High	R _T = 100Ω across P and N signals	–		–	mV
V _{CMOUT}	Common mode voltage	R _T = 100Ω across P and N signals	–		–	mV

GTY Transceiver Switching Characteristics

Consult www.xilinx.com/products/technology/high-speed-serial for further information.

Table 67: GTY Transceiver Performance

Symbol	Description	Output Divider	Speed Grade and V _{CCINT} Operating Voltages										Units
			0.90V		0.85V				0.72V				
			-3		-2		-1		-2		-1		
F _{GTymax}	GTY maximum line rate		32.75 ⁽¹⁾		28.21 ⁽¹⁾				12.5				Gb/s
F _{GTymin}	GTY minimum line rate		0.5		0.5				0.5				Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTyCRANGE}	CPLL line rate range ⁽²⁾	1	4.0	12.5	4.0	12.5	4.0	8.5	4.0	12.5	4.0	8.5	Gb/s
		2	2.0	6.25	2.0	6.25	2.0	4.25	2.0	6.25	2.0	4.25	Gb/s
		4	1.0	3.125	1.0	3.125	1.0	2.125	1.0	3.125	1.0	2.125	Gb/s
		8	0.5	1.5625	0.5	1.5625	0.5	1.0625	0.5	1.5625	0.5	1.0625	Gb/s
		16	N/A										Gb/s
		32	N/A										Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTyQRANGE1}	QPLL0 line rate range ⁽³⁾	1	19.6	32.75	19.6	28.21	N/A		19.6	28.21	N/A		Gb/s
		1	9.8	16.375	9.8	16.375	9.8	12.5	9.8	16.375	9.8	12.5	Gb/s
		2	4.9	8.1875	4.9	8.1875	4.9	8.1875	4.9	8.1875	4.9	8.1875	Gb/s
		4	2.45	4.09375	2.45	4.09375	2.45	4.09375	2.45	4.09375	2.45	4.09375	Gb/s
		8	1.225	2.04688	1.225	2.04688	1.225	2.04688	1.225	2.04688	1.225	2.04688	Gb/s
		16	0.6125	1.02344	0.6125	1.02344	0.6125	1.02344	0.6125	1.02344	0.6125	1.02344	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTyQRANGE2}	QPLL1 line rate range ⁽⁴⁾	1	16.0	26.0	16.0	26.0	N/A		16.0	26.0	N/A		Gb/s
		1	8.0	13.0	8.0	13.0	8.0	12.5	8.0	13.0	8.0	12.5	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{CPLL} RANGE	CPLL frequency range		2.0	6.25	2.0	6.25	2.0	4.25	2.0	6.25	2.0	4.25	GHz
F _{QPLL0} RANGE	QPLL0 frequency range		9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	GHz
F _{QPLL1} RANGE	QPLL1 frequency range		8.0	13.0	8.0	13.0	8.0	13.0	8.0	13.0	8.0	13.0	GHz

Notes:

1. GTY transceiver line rates are package limited: SFVB784 to 12.5 Gb/s; FFVA676, FFVD900, and FFVA1156 to 16.3 Gb/s.
2. The values listed are the rounded results of the calculated equation (2 x CPLL_Frequency)/Output_Divider.
3. The values listed are the rounded results of the calculated equation (2 x QPLL0_Frequency)/Output_Divider.
4. The values listed are the rounded results of the calculated equation (2 x QPLL1_Frequency)/Output_Divider.

Table 68: GTY Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	All Speed Grades	Units
$F_{GTYDRPCLK}$	GTYDRPCLK maximum frequency.		MHz

Table 69: GTY Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range.		60	–	820	MHz
T_{RCLK}	Reference clock rise time.	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time.	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle.	Transceiver PLL only	40	50	60	%

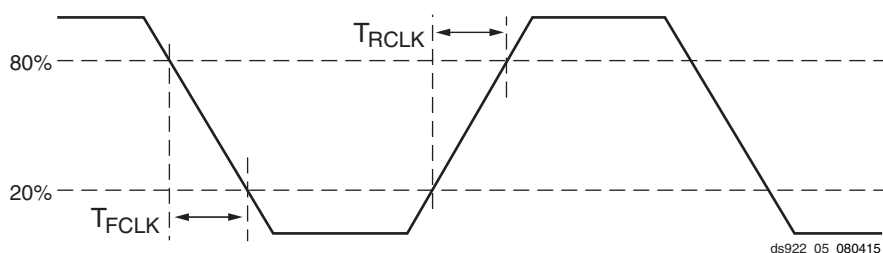


Figure 8: Reference Clock Timing Parameters

Table 70: GTY Transceiver Reference Clock Oscillator Selection Phase Noise Mask⁽¹⁾

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
QPLL _{REFCLKMASK}	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 156.25 MHz.	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 625 MHz.	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
CPLL _{REFCLKMASK}	CPLL reference clock select phase noise mask at REFCLK frequency = 156.25 MHz.	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 625 MHz.	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
		50 MHz	–	–	–144	

Notes:

- For reference clock frequencies not in this table, use the phase-noise mask for the nearest reference clock frequency.

Table 71: GTY Transceiver PLL/Lock Time Adaptation

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T _{LOCK}	Initial PLL lock.		–	–	1	ms
T _{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–			UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–			UI

Table 72: GTY Transceiver User Clock Switching Characteristics⁽¹⁾

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V _{CCINT} Operating Voltages					Units
				0.90V	0.85		0.72		
		Internal Logic	Interconnect Logic	-3	-2	-1	-2	-1	
F _{TXOUTPMA}	TXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	390.625	511.719	322.266	MHz
F _{RXOUTPMA}	RXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	390.625	511.719	322.266	MHz
F _{TXOUTPROGDIV}	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
F _{RXOUTPROGDIV}	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
F _{TXIN}	TXUSRCLK maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		64	64, 128	511.719	440.781	195.313	402.813	195.313	MHz
		20	20, 40	409.375	409.375	312.500	312.500	312.500	MHz
		40	40, 80	409.375	409.375	312.500	350.000	257.813	MHz
		80	80, 160	409.375	352.625	156.250	352.625	156.250	MHz
F _{RXIN}	RXUSRCLK maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		64	64, 128	511.719	440.781	195.313	402.813	195.313	MHz
		20	20, 40	409.375	409.375	312.500	312.500	312.500	MHz
		40	40, 80	409.375	409.375	312.500	350.000	257.813	MHz
		80	80, 160	409.375	352.625	156.250	352.625	156.250	MHz
F _{TXIN2}	TXUSRCLK2 maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		64	64, 128	511.719	440.781	195.313	402.813	195.313	MHz
		20	20, 40	409.375	409.375	312.500	312.500	312.500	MHz
		40	40, 80	409.375	409.375	312.500	350.000	257.813	MHz
		80	80, 160	409.375	352.625	156.250	352.625	156.250	MHz
F _{RXIN2}	RXUSRCLK2 maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		64	64, 128	511.719	440.781	195.313	402.813	195.313	MHz
		20	20, 40	409.375	409.375	312.500	312.500	312.500	MHz
		40	40, 80	409.375	409.375	312.500	350.000	257.813	MHz
		80	80, 160	409.375	352.625	156.250	352.625	156.250	MHz

Notes:

1. Clocking must be implemented as described in the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)).

Table 73: GTY Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTYTX}	Serial data rate range		0.500	–	F _{GTYMAX}	Gb/s
T _{RTX}	TX rise time	20%–80%	–		–	ps
T _{FTX}	TX fall time	80%–20%	–		–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–		ps
V _{TXOOBVDPP}	Electrical idle amplitude		–	–		mV
T _{TXOOBTRANSITION}	Electrical idle transition time		–	–		ns
T _{J32.75}	Total jitter ⁽²⁾⁽⁴⁾	32.75 Gb/s	–	–		UI
D _{J32.75}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–		UI
T _{J16.375}	Total jitter ⁽²⁾⁽⁴⁾	16.375 Gb/s	–	–		UI
D _{J16.375}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–		UI
T _{J12.5}	Total jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	–	–		UI
D _{J12.5}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–		UI
T _{J11.3}	Total jitter ⁽²⁾⁽⁴⁾	11.3 Gb/s	–	–		UI
D _{J11.3}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–		UI
T _{J10.3125_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	–	–		UI
D _{J10.3125_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–		UI
T _{J10.3125_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	10.3125 Gb/s	–	–		UI
D _{J10.3125_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–		UI
T _{J9.953}	Total jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	–	–		UI
D _{J9.953}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–		UI
T _{J9.8}	Total jitter ⁽²⁾⁽⁴⁾	9.8 Gb/s	–	–		UI
D _{J9.8}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–		UI
T _{J8.0_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	8.0 Gb/s	–	–		UI
D _{J8.0_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–		UI
T _{J8.0_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	8.0 Gb/s	–	–		UI
D _{J8.0_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–		UI
T _{J6.6_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	6.6 Gb/s	–	–		UI
D _{J6.6_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–		UI
T _{J5.0}	Total jitter ⁽³⁾⁽⁴⁾	5.0 Gb/s	–	–		UI
D _{J5.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–		UI
T _{J4.25}	Total jitter ⁽³⁾⁽⁴⁾	4.25 Gb/s	–	–		UI
D _{J4.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–		UI
T _{J3.75}	Total jitter ⁽³⁾⁽⁴⁾	3.75 Gb/s	–	–		UI
D _{J3.75}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–		UI
T _{J3.20}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁵⁾	–	–		UI
D _{J3.20}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–		UI
T _{J3.20L}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁶⁾	–	–		UI
D _{J3.20L}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–		UI
T _{J2.5}	Total jitter ⁽³⁾⁽⁴⁾	2.5 Gb/s ⁽⁷⁾	–	–		UI
D _{J2.5}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–		UI

Table 73: GTY Transceiver Transmitter Switching Characteristics (Cont'd)

Symbol	Description	Condition	Min	Typ	Max	Units
T _{J1.25}	Total jitter ⁽³⁾⁽⁴⁾	1.25 Gb/s ⁽⁸⁾	–	–		UI
D _{J1.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–		UI
T _{J500}	Total jitter ⁽³⁾⁽⁴⁾	500 Mb/s	–	–		UI
D _{J500}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–		UI

Notes:

- Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTY Quad) at maximum line rate.
- Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 10⁻¹².
- CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
- CPLL frequency at 1.6 GHz and TXOUT_DIV = 1.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.

Table 74: GTY Transceiver Receiver Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTYRX}	Serial data rate		0.500	–	F _{GTYMAX}	Gb/s
T _{RXELECIDLE}	Time for RXELECIDLE to respond to loss or restoration of data		–		–	ns
R _{XOOBVDPP}	OOB detect threshold peak-to-peak			–		mV
R _{XSSST}	Receiver spread-spectrum tracking ⁽¹⁾	Modulated at 33 kHz		–		ppm
R _{XRL}	Run length (CID)		–	–		UI
R _{XPPMTOL}	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s		–		ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s		–		ppm
		Bit rates > 8.0 Gb/s		–		ppm
SJ Jitter Tolerance⁽²⁾						
J _{T_SJ32.75}	Sinusoidal jitter (QPLL) ⁽³⁾	32.75 Gb/s		–	–	UI
J _{T_SJ16.375}	Sinusoidal jitter (QPLL) ⁽³⁾	16.375 Gb/s		–	–	UI
J _{T_SJ12.5}	Sinusoidal jitter (QPLL) ⁽³⁾	12.5 Gb/s		–	–	UI
J _{T_SJ11.3}	Sinusoidal jitter (QPLL) ⁽³⁾	11.3 Gb/s		–	–	UI
J _{T_SJ10.32_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	10.32 Gb/s		–	–	UI
J _{T_SJ10.32_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	10.32 Gb/s		–	–	UI
J _{T_SJ9.8}	Sinusoidal jitter (QPLL) ⁽³⁾	9.8 Gb/s		–	–	UI
J _{T_SJ8.0_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	8.0 Gb/s		–	–	UI
J _{T_SJ8.0_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	8.0 Gb/s		–	–	UI
J _{T_SJ6.6_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	6.6 Gb/s		–	–	UI
J _{T_SJ5.0}	Sinusoidal jitter (CPLL) ⁽³⁾	5.0 Gb/s		–	–	UI
J _{T_SJ4.25}	Sinusoidal jitter (CPLL) ⁽³⁾	4.25 Gb/s		–	–	UI
J _{T_SJ3.75}	Sinusoidal jitter (CPLL) ⁽³⁾	3.75 Gb/s		–	–	UI
J _{T_SJ3.2}	Sinusoidal jitter (CPLL) ⁽³⁾	3.2 Gb/s ⁽⁴⁾		–	–	UI
J _{T_SJ3.2L}	Sinusoidal jitter (CPLL) ⁽³⁾	3.2 Gb/s ⁽⁵⁾		–	–	UI
J _{T_SJ2.5}	Sinusoidal jitter (CPLL) ⁽³⁾	2.5 Gb/s ⁽⁶⁾		–	–	UI
J _{T_SJ1.25}	Sinusoidal jitter (CPLL) ⁽³⁾	1.25 Gb/s ⁽⁷⁾		–	–	UI
J _{T_SJ500}	Sinusoidal jitter (CPLL) ⁽³⁾	500 Mb/s		–	–	UI
SJ Jitter Tolerance with Stressed Eye⁽²⁾						
J _{T_TJSE3.2}	Total jitter with stressed eye ⁽⁸⁾	3.2 Gb/s		–	–	UI
J _{T_TJSE6.6}		6.6 Gb/s		–	–	UI
J _{T_SJSE3.2}	Sinusoidal jitter with stressed eye ⁽⁸⁾	3.2 Gb/s		–	–	UI
J _{T_SJSE6.6}		6.6 Gb/s		–	–	UI

Notes:

- Using RXOUT_DIV = 1, 2, and 4.
- All jitter values are based on a bit error ratio of 10⁻¹².
- The frequency of the injected sinusoidal jitter is 80 MHz.
- CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
- CPLL frequency at 1.6 GHz and RXOUT_DIV = 1.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
- Composite jitter with RX equalizer enabled. DFE disabled.

GTY Transceiver Electrical Compliance

The *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) contains recommended use modes that ensure compliance for the protocols listed in [Table 75](#). The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 75: GTY Transceiver Protocol List

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-4	IEEE 802.3-2012	25.78125	Compliant
28 Gb/s backplane	CEI-25G-LR	25–28.05	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11GSR, OIF-CEI-28G-MR	4.25–25.78125	Compliant
100GBASE-KR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
OTU4 (OTL4.4)	OIF-CEI-28G-VSR	27.952493	Compliant
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
PCIe Gen1, 2, 3	PCI Express base 3.0	2.5, 5.0, and 8.0	Compliant
SDI	SMPTE 424M-2006	0.27–2.97	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort (source only)	DP 1.2B CTS	1.62–5.4	Compliant
Fibre channel	FC-PI-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625 - 12.5	Compliant

Notes:

1. 25 dB loss at Nyquist without FEC.

GTY Transceiver Protocol Jitter Characteristics

For [Table 76](#) through [Table 81](#), the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) contains recommended settings for optimal usage of protocol specific characteristics.

Table 76: Gigabit Ethernet Protocol Characteristics (GTY Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	1250	–		UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250		–	UI

Table 77: XAUI Protocol Characteristics (GTY Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	3125	–		UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125		–	UI

Table 78: PCI Express Protocol Characteristics (GTY Transceivers)⁽¹⁾

Standard	Description	Condition	Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation						
PCI Express Gen 1	Total transmitter jitter		2500	–		UI
PCI Express Gen 2	Total transmitter jitter		5000	–		UI
PCI Express Gen 3 ⁽²⁾	Total transmitter jitter uncorrelated		8000	–		ps
	Deterministic transmitter jitter uncorrelated			–		ps
PCI Express Receiver High Frequency Jitter Tolerance						
PCI Express Gen 1	Total receiver jitter tolerance		2500		–	UI
PCI Express Gen 2 ⁽²⁾	Receiver inherent timing error		5000		–	UI
	Receiver inherent deterministic timing error				–	UI
PCI Express Gen 3 ⁽²⁾	Receiver sinusoidal jitter tolerance	0.03 MHz–1.0 MHz	8000		–	UI
		1.0 MHz–10 MHz		Note 3	–	UI
		10 MHz–100 MHz			–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. Using common REFCLK.
3. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20 dB/decade.

Table 79: CEI-6G and CEI-11G Protocol Characteristics (GTY Transceivers)

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter ⁽¹⁾	4976–6375	CEI-6G-SR	–		UI
		CEI-6G-LR	–		UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance ⁽¹⁾	4976–6375	CEI-6G-SR		–	UI
		CEI-6G-LR		–	UI
CEI-11G Transmitter Jitter Generation					
Total transmitter jitter ⁽²⁾	9950–11100	CEI-11G-SR	–		UI
		CEI-11G-LR/MR	–		UI
CEI-11G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance ⁽²⁾	9950–11100	CEI-11G-SR		–	UI
		CEI-11G-MR		–	UI
		CEI-11G-LR		–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.
2. Tested at line rate of 9950 Mb/s using 155.46875 MHz reference clock and 11100 Mb/s using 173.4375 MHz reference clock.

Table 80: SFP+ Protocol Characteristics (GTY Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
SFP+ Transmitter Jitter Generation				
Total transmitter jitter	9830.40 ⁽¹⁾	–		UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			
SFP+ Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	9830.40 ⁽¹⁾		–	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			

Notes:

1. Line rated used for CPRI over SFP+ applications.

Table 81: CPRI Protocol Characteristics (GTY Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter		–		UI
		–		UI
		–		UI
		–		UI
		–		UI
		–		UI
			–	Note 1
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance			–	UI
			–	UI
			–	UI
			–	UI
			–	UI
			–	UI
		Note 1	–	UI

Notes:

1. Tested per SFP+ specification, see [Table 80](#).

Integrated Interface Block for Interlaken

More information and documentation on solutions using the integrated interface block for Interlaken can be found at [UltraScale Interlaken](#). The *UltraScale Architecture and Product Overview* ([DS890](#)) lists how many blocks are in each Kintex UltraScale+ FPGA.

Table 82: Maximum Performance for Interlaken Designs

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3 ⁽¹⁾		-2 ⁽¹⁾		-1		-2 ⁽¹⁾		-1		
F _{RX_SERDES_CLK}	Receive serializer/deserializer clock	440.79		440.79				195.32				MHz
F _{TX_SERDES_CLK}	Transmit serializer/deserializer clock	440.79		440.79				195.32				MHz
F _{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00				250.00				MHz
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{CORE_CLK}	Interlaken core clock	300.00 ⁽²⁾		300.00 ⁽²⁾		300.00	322.27	300.00 ⁽²⁾	429.69	300.00	322.27	MHz
		460.00 ⁽³⁾		460.00 ⁽³⁾				412.50 ⁽³⁾				MHz
F _{LBUS_CLK}	Interlaken local bus clock	300.00	349.52	300.00	349.52	300.00	322.27	300.00	349.52	300.00	322.27	MHz

Notes:

1. Kintex UltraScale+ FPGAs in the SFVB784, FFVA676, and FFVA1156 packages are only supported using the 12 x 12.5G Interlaken configuration. See [Table 67](#) for the F_{GTYMAX} description.
2. The minimum value for CORE_CLK is 300 MHz for the 12 x 12.5G Interlaken configuration.
3. The minimum value for CORE_CLK is 412.5 MHz for the 6 x 25.78125G Interlaken configuration.

Integrated Interface Block for 100G Ethernet MAC and PCS

More information and documentation on solutions using the integrated 100 Gb/s Ethernet block can be found at [UltraScale Integrated 100G Ethernet MAC/PCS](#). The *UltraScale Architecture and Product Overview (DS890)* lists how many blocks are in each Kintex UltraScale+ FPGA.

Table 83: Maximum Performance for 100G Ethernet Designs

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2 ⁽¹⁾	-1	-2	-1	
F _{TX_CLK}	Transmit clock	390.625	390.625	322.223	322.223	322.223	MHz
F _{RX_CLK}	Receive clock	390.625	390.625	322.223	322.223	322.223	MHz
F _{RX_SERDES_CLK}	Receive serializer/deserializer clock	390.625	390.625	322.223	322.223	322.223	MHz
F _{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	250.00	250.00	250.00	MHz

Notes:

1. The maximum clock frequency of 390.625 MHz only applies to the CAUI-10 interface. The maximum clock frequency for the CAUI-4 interface is 322.223 MHz.

Integrated Interface Block for PCI Express Designs

More information and documentation on solutions for PCI Express designs can be found at [PCI Express](#). The *UltraScale Architecture and Product Overview (DS890)* lists how many blocks are in each Kintex UltraScale+ FPGA.

Table 84: Maximum Performance for PCI Express Designs⁽¹⁾⁽²⁾

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
F _{PIPECLK}	Pipe clock maximum frequency.	250.00	250.00	250.00	250.00	250.00	MHz
F _{CORECLK}	Core clock maximum frequency.	500.00	500.00	500.00	250.00	250.00	MHz
F _{DRPCLK}	DRP clock maximum frequency.	250.00	250.00	250.00	250.00	250.00	MHz
F _{MCAPCLK}	MCAP clock maximum frequency.	125.00	125.00	125.00	125.00	125.00	MHz

Notes:

1. PCI Express Gen4 operation is supported for x1, x2, x4, and x8 widths.
2. PCI Express Gen4 operation is supported in -2I and -3E speed grades.

System Monitor Specifications

Table 85: System Monitor Specifications

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
$V_{CCADC} = 1.8V \pm 3\%$, $V_{REFP} = 1.25V$, $V_{REFN} = 0V$, $ADCCLK = 5.2\text{ MHz}$, $T_j = -40^\circ\text{C}$ to 100°C , typical values at $T_j = 40^\circ\text{C}$						
ADC Accuracy⁽¹⁾						
Resolution			10	–	–	Bits
Integral nonlinearity ⁽²⁾	INL		–	–	± 1.5	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	± 1	LSBs
Offset error		Offset calibration enabled	–	–	± 2	LSBs
Gain error			–	–	± 0.4	%
Sample rate			–	–	0.2	MS/s
RMS code noise		External 1.25V reference	–	–	1	LSBs
		On-chip reference	–	1	–	LSBs
ADC Accuracy at Extended Temperatures						
Resolution		$T_j = -55^\circ\text{C}$ to 125°C	10	–	–	Bits
Integral nonlinearity	INL	$T_j = -55^\circ\text{C}$ to 125°C	–	–	± 1	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic $T_j = -55^\circ\text{C}$ to 125°C	–	–	± 1	
Analog Inputs⁽²⁾						
ADC input ranges		Unipolar operation	0	–	1	V
		Bipolar operation	–0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum external channel input ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	–0.1	–	V_{CCADC}	V
On-Chip Sensor Accuracy						
Temperature sensor error ⁽¹⁾		$T_j = -40^\circ\text{C}$ to 100°C (with external REF)	–	–	± 4	$^\circ\text{C}$
		$T_j = -55^\circ\text{C}$ to 125°C (with external REF)	–	–	± 4.5	$^\circ\text{C}$
		$T_j = -40^\circ\text{C}$ to 100°C (with internal REF)	–	–	± 5	$^\circ\text{C}$
		$T_j = -55^\circ\text{C}$ to 125°C (with internal REF)	–	–	± 6.5	$^\circ\text{C}$

Table 85: System Monitor Specifications (Cont'd)

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Supply sensor error ⁽³⁾		Supply voltages 0.72V to 1.2V, $T_j = -40^\circ\text{C}$ to 100°C (with external REF)	–	–	± 0.5	%
		Supply voltages 0.72V to 1.2V, $T_j = -55^\circ\text{C}$ to 125°C (with external REF)	–	–	± 1.0	%
		All other supply voltages, $T_j = -40^\circ\text{C}$ to 100°C (with external REF)	–	–	± 1.0	%
		All other supply voltages, $T_j = -55^\circ\text{C}$ to 125°C (with external REF)	–	–	± 2.0	%
		Supply voltages 0.72V to 1.2V, $T_j = -40^\circ\text{C}$ to 100°C (with internal REF)	–	–	± 1.0	%
		Supply voltages 0.72V to 1.2V, $T_j = -55^\circ\text{C}$ to 125°C (with internal REF)	–	–	± 2.0	%
		All other supply voltages, $T_j = -40^\circ\text{C}$ to 100°C (with internal REF)	–	–	± 1.5	%
		All other supply voltages, $T_j = -55^\circ\text{C}$ to 125°C (with internal REF)	–	–	± 2.5	%
Conversion Rate⁽⁴⁾						
Conversion time—continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	Cycles
Conversion time—event	t_{CONV}	Number of ADCCLK cycles	–	–	21	Cycles
DRP clock frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC clock frequency	ADCCLK	Derived from DCLK	1	–	5.2	MHz
DCLK duty cycle			40	–	60	%
SYSMON Reference⁽⁵⁾						
External reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-chip reference		Ground V_{REFP} pin to AGND, $T_j = -40^\circ\text{C}$ to 100°C	1.2375	1.25	1.2625	V
		Ground V_{REFP} pin to AGND, $T_j = -55^\circ\text{C}$ to 125°C	1.225	1.25	1.275	V

Notes:

1. ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
2. See the *Analog Input* section in the *UltraScale Architecture System Monitor User Guide* ([UG580](#)).
3. Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.
4. See the *Adjusting the Acquisition Settling Time* section in the *UltraScale Architecture System Monitor User Guide* ([UG580](#)).
5. Any variation in the reference voltage from the nominal $V_{\text{REFP}} = 1.25\text{V}$ and $V_{\text{REFN}} = 0\text{V}$ will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by $\pm 4\%$ is permitted.

SYSMON I2C/PMBus Interfaces

Table 86: SYSMON I2C Fast Mode Interface Switching Characteristics⁽¹⁾

Symbol	Description	Min	Max	Units
T_{SMFCKL}	SCL Low time	1.3	–	μ s
T_{SMFCKH}	SCL High time	0.6	–	μ s
T_{SMFCKO}	SDAO clock-to-out delay	–	900	ns
T_{SMFDCK}	SDAI setup time	100	–	ns
F_{SMFCLK}	SCL clock frequency	–	400	kHz

Notes:

1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

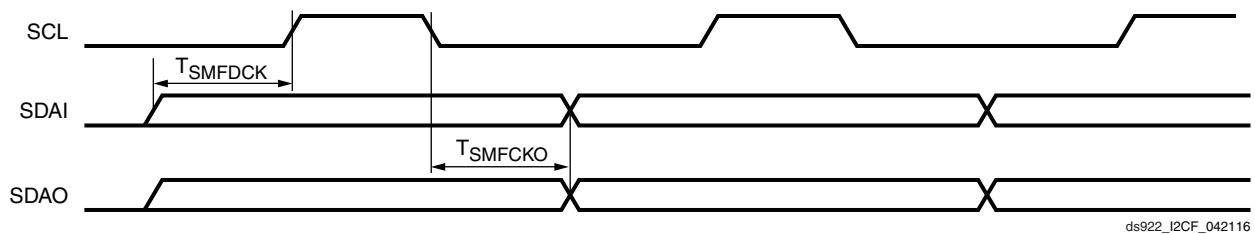


Figure 9: SYSMON I2C Fast Mode Interface Timing Diagram

Table 87: SYSMON I2C Standard Mode Interface Switching Characteristics⁽¹⁾

Symbol	Description	Min	Max	Units
T_{SMSCKL}	SCL Low time	4.7	–	μ s
T_{SMSCKH}	SCL High time	4.0	–	μ s
T_{SMSCKO}	SDAO clock-to-out delay	–	3450	ns
T_{SMSDCK}	SDAI setup time	250	–	ns
F_{SMSCLK}	SCL clock frequency	–	100	kHz

Notes:

1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

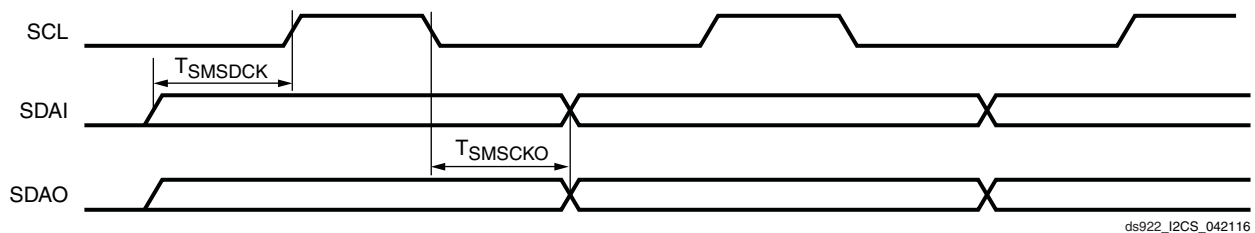


Figure 10: SYSMON I2C Standard Mode Interface Timing Diagram

Configuration Switching Characteristics

Table 88: Configuration Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Power-up Timing Characteristics							
T _{PL}	Program latency.	7.5	7.5	7.5	7.5	7.5	ms, Max
T _{POR}	Power-on reset (40 ms ramp rate time).	57	57	57	57	57	ms, Max
		0	0	0	0	0	ms, Min
	Power-on reset with POR override (2 ms ramp rate time).	15	15	15	15	15	ms, Max
		5	5	5	5	5	ms, Min
T _{PROGRAM}	Program pulse width.	250	250	250	250	250	ns, Min
CCLK Output (Master Mode)							
T _{ICCK}	Master CCLK output delay from INIT_B.	150	150	150	150	150	ns, Min
T _{MCCKL} ⁽¹⁾	Master CCLK clock Low time duty cycle.	40/60	40/60	40/60	40/60	40/60	%, Min/Max
T _{MCCKH}	Master CCLK clock High time duty cycle.	40/60	40/60	40/60	40/60	40/60	%, Min/Max
F _{MCCK}	Master CCLK frequency.	150	150	150	150	150	MHz, Max
F _{MCCK_START}	Master CCLK frequency at start of configuration.	3.00	3.00	3.00	3.00	3.00	MHz, Typ
F _{MCCKTOL}	Frequency tolerance, master mode with respect to nominal CCLK.	±15	±15	±15	±15	±15	%, Max
EMCCLK Input (Master Mode)							
T _{EMCCKL}	External master CCLK Low time.	2.5	2.5	2.5	2.5	2.5	ns, Min
T _{EMCCKH}	External master CCLK High time.	2.5	2.5	2.5	2.5	2.5	ns, Min
F _{EMCCK}	External master CCLK frequency.	150	150	150	150	150	MHz, Max
Internal Configuration Access Port							
F _{ICAPCK}	Internal configuration access port (ICAPE3).	200	200	200	175	175	MHz, Max
Slave Serial Mode Programming Switching							
T _{DCCK} /T _{CCKD}	D _{IN} setup/hold.	3.0/0	3.0/0	3.0/0	3.5/0	3.5/0	ns, Min
T _{CCO}	D _{OUT} clock to out.	8	8	8	8	8	ns, Max
SelectMAP Mode Programming Switching							
T _{SMDCCCK} /T _{SMCCKD}	D[31:00] setup/hold.	3.5/0	3.5/0	3.5/0	4.0/0	4.0/0	ns, Min
T _{SMCSCCK} /T _{SMCCKCS}	CSI_B setup/hold.	4.0/0	4.0/0	4.0/0	4.5/0	4.5/0	ns, Min
T _{SMWCCCK} /T _{SMCCKW}	RDWR_B setup/hold.	10.0/0	10.0/0	10.0/0	10.0/0	10.0/0	ns, Min
T _{SMCKCSO}	CSO_B clock to out (330Ω pull-up resistor required).	7	7	7	7	7	ns, Max
T _{SMCO}	D[31:00] clock to out in readback.	8	8	8	8	8	ns, Max
F _{RBCCK}	Readback frequency.	125	125	125	125	125	MHz, Max

Table 88: Configuration Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Boundary-Scan Port Timing Specifications							
T _{TAPTCK} /T _{TCKTAP}	TMS and TDI setup/hold.	3.0/ 2.0	3.0/ 2.0	3.0/ 2.0	3.0/ 2.0	3.0/ 2.0	ns, Min
T _{TCKTDO}	TCK falling edge to TDO output.	7	7	7	7	7	ns, Max
F _{TCK}	TCK frequency.	66	66	66	66	66	MHz, Max
BPI Master Flash Mode Programming Switching							
T _{BPICCO}	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out.	10	10	10	10	10	ns, Max
T _{BPIDCC} /T _{BPICCD}	D[15:00] setup/hold.	3.5/0	3.5/0	3.5/0	4.0/0	4.0/0	ns, Min
SPI Master Flash Mode Programming Switching							
T _{SPIDCC} /T _{SPICCD}	D[03:00] setup/hold.	3.0/0	3.0/0	3.0/0	3.5/0	3.5/0	ns, Min
T _{SPIDCC} /T _{SPICCD}	D[07:04] setup/hold.	3.5/0	3.5/0	3.5/0	4.0/0	4.0/0	ns, Min
T _{SPICCM}	MOSI clock to out.	8.0	8.0	8.0	8.0	8.0	ns, Max
T _{SPICFC}	FCS_B clock to out.	8.0	8.0	8.0	8.0	8.0	ns, Max
DNA Port Switching							
F _{DNACK}	DNA port frequency.	200	200	200	175	175	MHz, Max
STARTUPE3 Ports							
T _{USRCCLKO}	STARTUPE3 USRCCLKO input port to CCLK pin output delay.	1.00/ 6.00	1.00/ 6.70	1.00/ 7.50	1.00/ 7.50	1.00/ 7.50	ns, Min/Max
T _{DO}	DO[3:0] ports to D03-D00 pins output delay.	1.00/ 6.70	1.00/ 7.70	1.00/ 8.40	1.00/ 8.40	1.00/ 8.40	ns, Min/Max
T _{DTS}	DTS[3:0] ports to D03-D00 pins 3-state delays.	1.00/ 7.30	1.00/ 8.30	1.00/ 9.00	1.00/ 9.00	1.00/ 9.00	ns, Min/Max
T _{FCSBO}	FCSBO port to FCS_B pin output delay.	1.00/ 6.90	1.00/ 8.00	1.00/ 8.60	1.00/ 8.60	1.00/ 8.60	ns, Min/Max
T _{FCSBTS}	FCSBTS port to FCS_B pin 3-state delay.	1.00/ 6.90	1.00/ 8.00	1.00/ 8.60	1.00/ 8.60	1.00/ 8.60	ns, Min/Max
T _{USRDONEO}	USRDONEO port to DONE pin output delay.	1.00/ 8.50	1.00/ 9.60	1.00/ 10.40	1.00/ 10.40	1.00/ 10.40	ns, Min/Max
T _{USRDONETS}	USRDONETS port to DONE pin 3-state delay.	1.00/ 8.50	1.00/ 9.60	1.00/ 10.40	1.00/ 10.40	1.00/ 10.40	ns, Min/Max
T _{DI}	D03-D00 pins to DI[3:0] ports input delay.	0.5/ 2.6	0.5/ 3.1	0.5/ 3.5	0.5/ 3.5	0.5/ 3.5	ns, Min/Max
F _{CFGMCLK}	STARTUPE3 CFGMCLK output frequency.	50	50	50	50	50	MHz, Typ
F _{CFGMCLKTOL}	STARTUPE3 CFGMCLK output frequency tolerance.	±15	±15	±15	±15	±15	%, Max
T _{DCI_MATCH}	Specifies a stall in the startup cycle until the digitally controlled impedance (DCI) match signals are asserted.	4	4	4	4	4	ms, Max

Notes:

- When the CCLK is sourced from the EMCCLK pin with a divide-by-one setting, the external EMCCLK must meet this duty-cycle requirement.

eFUSE Programming Conditions

Table 89: eFUSE Programming Conditions⁽¹⁾

Symbol	Description	Min	Typ	Max	Units
I_{PLFS}	V_{CCAUX} supply current.	–	–	115	mA
t_j	Temperature range.	–40	–	125	°C

Notes:

- Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
05/09/2016	1.1	In Table 1 revised V_{IN} for HP I/O banks. Updated Note 5 in Table 3 . Added values to Table 7 . Added MIPI_DPHY_DCI to Table 9 , Table 10 , and Table 12 . Updated and added notes in Table 18 and Table 19 . Updated Table 20 speed specifications for Vivado Design Suite 2016.1. Removed Table 23 , <i>Video Codec Unit Performance</i> . Updated Table 24 . Expanded and updated Table 26 . Updated Table 27 and Table 28 . Updated Table 30 and Table 31 with MIPI D-PHY values. Updated the tables in the I/O Standard Adjustment Measurement Methodology section. In Table 32 , added the Block RAM and FIFO Clock-to-Out Delays section. Updated Table 39 to Table 43 . Revised the symbol names in Table 42 . Revised typical values in Table 47 . Updated the -2 (0.72V) and -1 (0.72V) values in Table 49 . Added Table 52 and Table 70 . Added Note 2 to Table 64 . Revised Table 72 . Revised data and added notes to Table 67 , Table 82 , and Table 83 . Revised INL in Table 85 . Added notes to Table 86 and Table 87 . Many revised sections in Table 88 .
11/24/2015	1.0	Initial Xilinx release.

Notice of Disclaimer

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx's limited warranty, please refer to Xilinx's Terms of Sale which can be viewed at www.xilinx.com/legal.htm#tos; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx's Terms of Sale which can be viewed at www.xilinx.com/legal.htm#tos.

Automotive Applications Disclaimer

XILINX PRODUCTS ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE, OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS APPLICATIONS RELATED TO: (I) THE DEPLOYMENT OF AIRBAGS, (II) CONTROL OF A VEHICLE, UNLESS THERE IS A FAIL-SAFE OR REDUNDANCY FEATURE (WHICH DOES NOT INCLUDE USE OF SOFTWARE IN THE XILINX DEVICE TO IMPLEMENT THE REDUNDANCY) AND A WARNING SIGNAL UPON FAILURE TO THE OPERATOR, OR (III) USES THAT COULD LEAD TO DEATH OR PERSONAL INJURY. CUSTOMER ASSUMES THE SOLE RISK AND LIABILITY OF ANY USE OF XILINX PRODUCTS IN SUCH APPLICATIONS.